NOVATEK
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Data Sheet

NT7538

132 X 65 RAM-Map STN LCD Controller/Driver

V0.01

Preliminary

Revision History

NT7538 Specification Revision History		
Version	**Content**	**Date**
0.00	Original	August 2005
0.01	1. Add pad location information. 2. Modify application information for LCD panel. 3. Modify application information for pin connection to MPU. 4. Modify pad configuration. 5. Modify description of RESET.	October 2005

Features

- 132 x 65-dot graphics display LCD controller/driver for black/white STN LCD
- RAM capacity: 132 x 65 = 8,580 bits
- 8-bit parallel bus interface for both 8080 and 6800 series,
  4-wire Serial Peripheral Interface (SPI)
- Direct RAM data display using the display data RAM.
  When RAM data bit is 0, it is not displayed. When RAM data bit is 1, it is displayed.
  (At normal display)
- Many command functions:
  Read/Write display data, display ON/OFF, Normal/Reverse display, page address set, display start line set, LCD bias set, electronic contrast controls, V0 voltage regulation internal resistor ratio set, read modify write, segment driver direction select, power save.
- Other command functions:
  Partial display, partial start line set, N-Line inversion.
- Power supply voltage:
  - VDD = 1.8 ~ 3.6 V
  - VDD2 = 1.8 ~ 3.6 V
  - V0 = 4.0 ~ 14.2 V
  - VOUT = 14.2 V Max.
- 2X / 3X / 4X / 5X on chip DC-DC converter
- On chip LCD driving voltage generator or external power supply selectable
- 64-step contrast adjuster and on chip voltage follower
- On chip oscillation and hardware reset

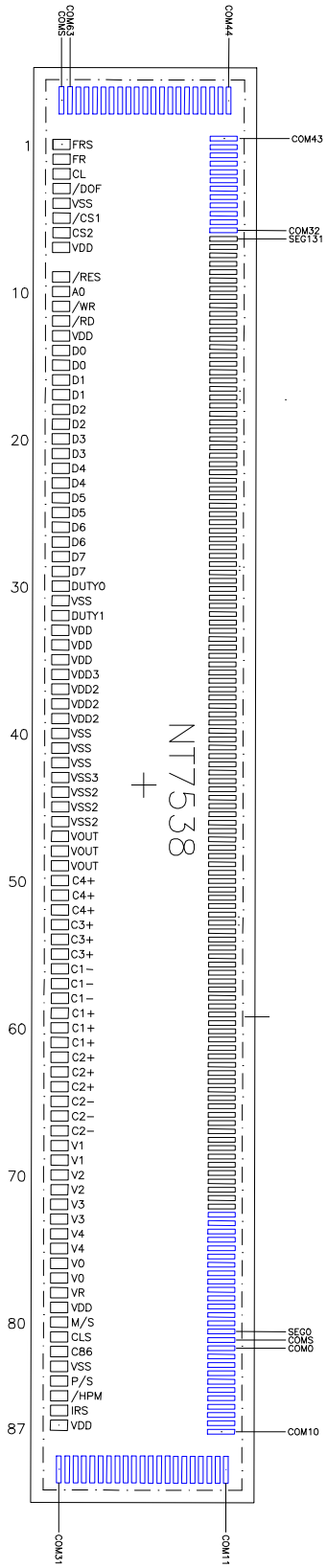
General Description

The NT7538 is a single-chip LCD driver for dot-matrix liquid crystal displays, which is directly connectable to a microcomputer bus. It accepts 8-bit parallel or serial display data directly sent from a microcomputer and stores it in an on-chip display RAM. It generates an LCD drive signal independent of the microprocessor clock.

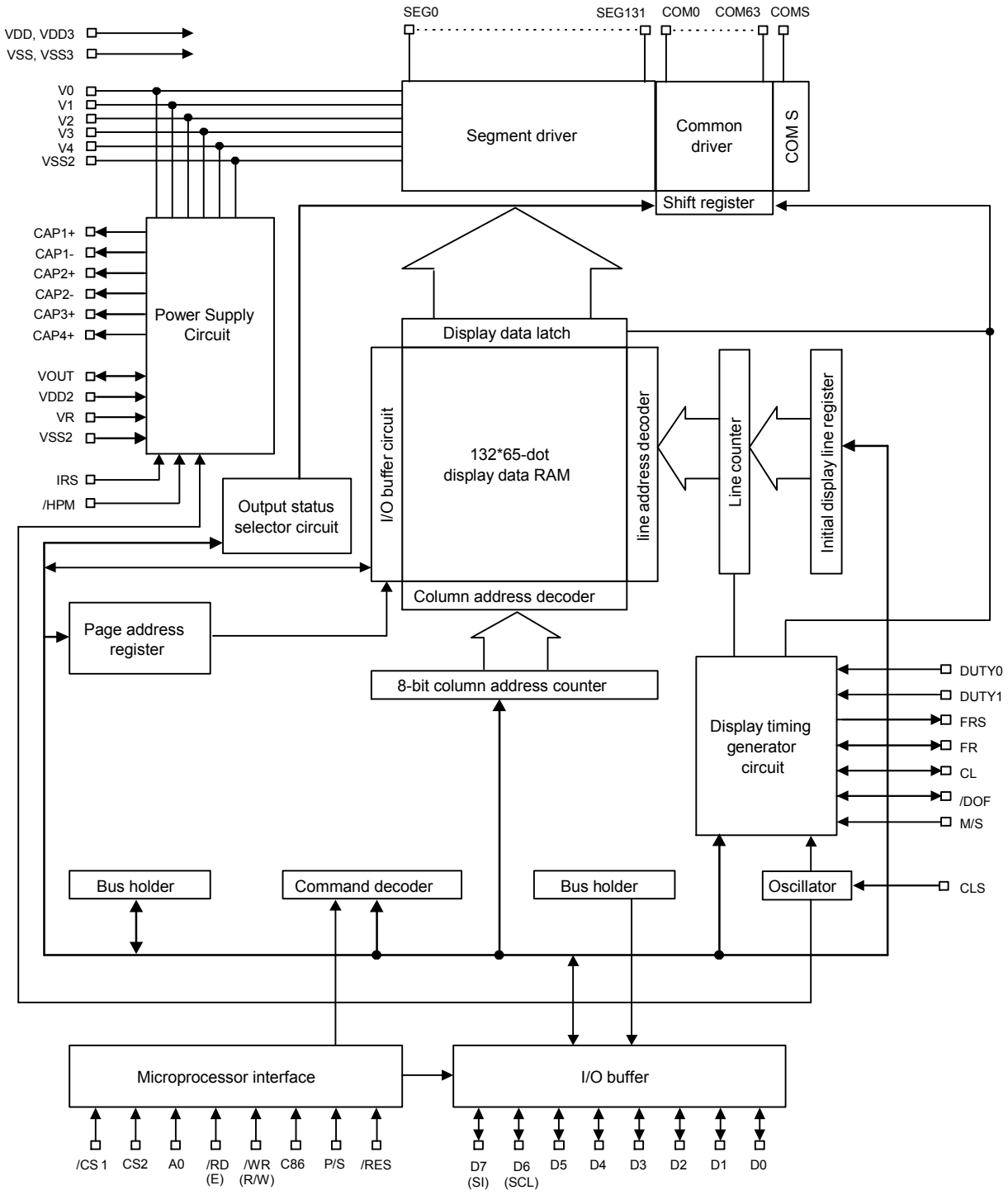
The set of the on-chip display RAM of 65 x 132 bits and a one-to-one correspondence between LCD panel pixel dots and on-chip RAM bits permits implementation of displays with a high degree of freedom. The NT7538 contain 65 common output circuits and 132 segment output circuits, so that a single chip of NT7538 can make maximum 65 x 132 or 49 x 132 or 33 x 132 dots display with the pad option (DUTY1, DUTY0).

No external operation clock is required for RAM read/write operations. Accordingly, this driver can be operated with a minimum current consumption and its on-board low-current-consumption liquid crystal power supply can implement a high-performance handy display system with minimum current consumption and the smallest LSI configuration.

Pad Configuration



Block Diagram



Pad Descriptions

Power Supply

<table>
<tr><th>Pad No.</th><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td>33~35</td><td>VDD</td><td rowspan="2">Supply</td><td rowspan="2">Power supply input. These pads must be connected to each other.</td></tr>
<tr><td>36</td><td>VDD3</td></tr>
<tr><td>37~39</td><td>VDD2</td><td>Supply</td><td>These are the power supply pads for the step-up voltage circuit for the LCD. These pads must be connected to each other.</td></tr>
<tr><td>8,13,79,87</td><td>VDD</td><td>O</td><td>Power supply output for pad option</td></tr>
<tr><td>40~42</td><td>VSS</td><td rowspan="2">Supply</td><td rowspan="2">Ground. These pads must be connected to each other.</td></tr>
<tr><td>43</td><td>VSS3</td></tr>
<tr><td>44~46</td><td>VSS2</td><td>Supply</td><td>Ground. These pads must be connected to each other.</td></tr>
<tr><td>5,31,83</td><td>VSS</td><td>O</td><td>Ground output for pad option.</td></tr>
<tr><td>76,77</td><td>V0</td><td rowspan="5">I/O</td><td rowspan="5">LCD driver supplies voltages. The voltage determined by the LCD cell is impedance-converted by a resistive driver or an operation amplifier for application. Voltages should be according to the following relationship:
V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS2
When the on-chip operating power circuit is on, the following voltages are supplied to V1 to V4 by the on-chip power circuit. Voltage selection is performed by the LCD Bias Set command.
<table>
<tr><td>LCD bias</td><td>V1</td><td>V2</td><td>V3</td><td>V4</td></tr>
<tr><td>1/4 bias</td><td>3/4V0</td><td>2/4V0</td><td>2/4V0</td><td>1/4V0</td></tr>
<tr><td>1/5 bias</td><td>4/5V0</td><td>3/5V0</td><td>2/5V0</td><td>1/5V0</td></tr>
<tr><td>1/6 bias</td><td>5/6V0</td><td>4/6V0</td><td>2/6V0</td><td>1/6V0</td></tr>
<tr><td>1/7 bias</td><td>6/7V0</td><td>5/7V0</td><td>2/7V0</td><td>1/7V0</td></tr>
<tr><td>1/8 bias</td><td>7/8V0</td><td>6/8V0</td><td>2/8V0</td><td>1/8V0</td></tr>
<tr><td>1/9 bias</td><td>8/9V0</td><td>7/9V0</td><td>2/9V0</td><td>1/9V0</td></tr>
</table></td></tr>
<tr><td>68,69</td><td>V1</td></tr>
<tr><td>70,71</td><td>V2</td></tr>
<tr><td>72,73</td><td>V3</td></tr>
<tr><td>74,75</td><td>V4</td></tr>
</table>

Note: VDD and VDD3 pads must be connected together.

LCD Power Supply

Pad No.	Designation	I/O	Description
56~58	C1-	O	Capacitor 1- pad for internal DC/DC voltage converter.
59~61	C1+	O	Capacitor 1+ pad for internal DC/DC voltage converter.
65~67	C2-	O	Capacitor 2- pad for internal DC/DC voltage converter.
62~64	C2+	O	Capacitor 2+ pad for internal DC/DC voltage converter.
53~55	C3+	O	Capacitor 3+ pad for internal DC/DC voltage converter.
50~52	C4+	O	Capacitor 4+ pad for internal DC/DC voltage converter.
47~49	VOUT	I/O	DC/DC voltage converter output
78	VR	I	Voltage adjustment pad. Applies voltage between V0 and VSS using a resistive divider.

Configuration Pad

Pad No.	Designation	I/O	Description
30 32	DUTY0 DUTY1	I	Select the maximum LCD driver duty

DUTY1	DUTY0	LCD driver duty
0	0	1/33
0	1	1/49
1	*	1/65

System Bus Connection

Pad No.	Designation	I/O	Description
14,15 16,17 18,19 20,21 22,23 24,25 26,27 28,29	D0 D1 D2 D3 D4 D5 D6 (SCL) D7 (SI)	I/O	This is an 8-bit bi-directional data bus that connects to an 8-bit or 16-bit standard MPU data bus. When the serial interface is selected (P/S="L"), then D7 serves as the serial data input terminal (SI) and D6 serves as the serial clock input terminal (SCL). When the serial interface is selected, fix D0~D5 pads to VDD or VSS level. When the chip select is inactive, D0 to D7 are set to high impedance.
10	A0	I	This is connected to the least significant bit of the normal MPU address bus, and it determines whether the data bits are data or a command. A0 = "H": Indicate that D0 to D7 are display data A0 = "L": Indicates that D0 to D7 are control data
9	/RES	I	When /RES is set to "L", the settings are initialized. The reset operation is performed by the /RES signal level
6 7	/CS1 CS2	I	This is the chip select signal. When /CS1="L" and CS2="H", then the chip select becomes active, and data/command I/O is enabled.
12	/RD (E)	I	When connected to an 8080 MPU, it is active LOW. This pad is connected to the /RD signal of the 8080MPU, and the NT7538 data bus is in an output status when this signal is "L". When connected to a 6800 Series MPU, this is active HIGH. This is used as an enable clock input of the 6800 series MPU
11	/WR (R/W)	I	When connected to an 8080 MPU, this is active LOW. This terminal connects to the 8080 MPU /WR signal. The signals on the data bus are latched at the rising edge of the /WR signal. When connected to a 6800 Series MPU, this is the read/write control signal input terminal. When R/W = "H": Read When R/W = "L": Write
82	C86	I	This is the MPU interface switch terminal C86 = "H": 6800 Series MPU interface C86 = "L": 8080 Series MPU interface

System Bus Connection (continuous)

<table>
<tr><th>Pad No.</th><th>Designation</th><th>I/O</th><th>Description</th></tr>
<tr><td>84</td><td>P/S</td><td>I</td><td>This is the parallel data input/serial data input switch terminal
P/S = “H”: Parallel data input
P/S = “L”: Serial data input
The following applies depending on the P/S status:
<table>
<tr><td>P/S</td><td>Data/Command</td><td>Data</td><td>Read/Write</td><td>Serial Clock</td></tr>
<tr><td>“H”</td><td>A0</td><td>D0 to D7</td><td>/RD, /WR</td><td>-</td></tr>
<tr><td>“L”</td><td>A0</td><td>SI (D7)</td><td>Write only</td><td>SCL (D6)</td></tr>
</table>
When P/S = “L”, fix D0~D5 pads to VDD or VSS level. /RD (E) and /WR (R/W) are fixed to either “H” or “L”. With serial data input, RAM display data reading is not supported.</td></tr>
<tr><td>81</td><td>CLS</td><td>I</td><td>Terminal to select whether enable or disable the display clock internal oscillator circuit.
CLS = “H”: Internal oscillator circuit for display is enabled
CLS = “L”: Internal oscillator circuit for display is disabled
(requires external input)
When CLS = “L”, input the display clock through the CL pad.</td></tr>
<tr><td>80</td><td>M/S</td><td>I</td><td>This terminal selects the master/slave operation for the NT7538 chips. Master operation outputs the timing signals that are required for the LCD display, while slave operation inputs the timing signals required for the liquid crystal display, synchronizing the liquid crystal display system.</td></tr>
<tr><td>3</td><td>CL</td><td>I/O</td><td>This is the display clock input terminal. When the NT7538 chips are used in master/slave mode, the various CL terminals must be connected.</td></tr>
<tr><td>2</td><td>FR</td><td>I/O</td><td>This is the liquid crystal alternating current signal I/O terminal
M/S = “H”: Output
M/S = “L”: Input
When the NT7538 chip is used in master/slave mode, the various FR terminals must be connected.</td></tr>
<tr><td>4</td><td>/DOF</td><td>I/O</td><td>This is the liquid crystal display blanking control terminal.
M/S = “H”: Output
M/S = “L”: Input
When the NT7538 chip is used in master/slave mode, the various /DOF terminals must be connected.</td></tr>
<tr><td>1</td><td>FRS</td><td>O</td><td>This is the output terminal for the static drive. This terminal is only enabled when the static indicator display is ON in master operation mode, and is used in conjunction with the FR terminal</td></tr>
</table>

System Bus Connection (continuous)

Pad No.	Designation	I/O	Description
86	IRS	I	This terminal selects the resistors for the V0 voltage level adjustment. IRS = "H", Use the internal resistors IRS = "L", Do not use the internal resistors The V0 voltage level is regulated by an external resistive voltage divider attached to the VR terminal. This pad is enabled only when the master operation mode is selected. It is fixed to either "H" or "L" when the slave operation mode is selected
85	/HPM	I	This is the power control terminal for the power supply circuit for liquid crystal drive. /HPM = "H", Normal power mode /HPM = "L", High power mode This pad is enabled only when the master operation mode is selected and it is fixed to either "H" or "L" when the slave operation mode is selected.

Liquid Crystal Drive Pads

Pad No.	Designation	I/O	Description
121~252	SEG0 - 131	O	Segment signal output for LCD display.
88~119 253~284	COM31 – 0 COM32 – 63	O	Common signal output for LCD display. When in master/slave mode, the same signal is output by both master and slave
120,285	COMS	O	These are the COM output terminals for the indicator. Both terminals output the same signal. Do not connect these terminals if they are not used. When in master/slave mode, the same signal is output by both master and slave.

Functional Descriptions

Microprocessor Interface

Interface Type Selection

The NT7538 can transfer data via 8-bit bi-directional data bus (D7 to D0) or via serial data input (SI). When high or low is selected for the parity of P/S pad either 8-bit parallel data input or serial data input can be selected as shown in Table 1. When serial data input is selected, the RAM data cannot be read out.

Table 1

P/S	Type	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D0 to D5
H	Parallel Input	/CS1	CS2	A0	/RD	/WR	C86	D7	D6	D0 to D5
L	Serial Input	/CS1	CS2	A0	-	-	-	SI	SCL	-

"-" Must always be high or low

Parallel Interface

When the NT7538 selects parallel input (P/S = high), the 8080 series microprocessor or 6800 series microprocessor can be selected by causing the C86 pad to go high or low as shown in Table 2.

Table 2

C86	Type	/CS1	CS2	A0	/RD	/WR	D0 to D7
H	6800 microprocessor bus	/CS1	CS2	A0	E	R/W	D0 to D7
L	8080 microprocessor bus	/CS1	CS2	A0	/RD	/WR	D0 to D7

Data Bus Signals

The NT7538 identifies the data bus signal according to A0, E, R/W (/RD, /WR) signals.

Table 3

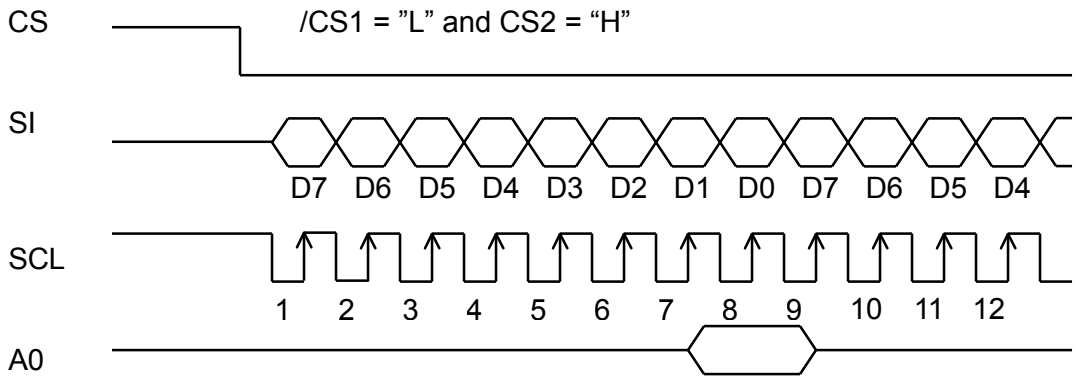
Common	6800 processor	8080 processor		Function
A0	(R/W)	/RD	/WR	
1	1	0	1	Reads display data
1	0	1	0	Writes display data
0	1	0	1	Reads status
0	0	1	0	Writes control data in internal register. (Command)

Serial Interface

When the serial interface has been selected (P/S = “L”), then when the chip is in active state (/CS1 = “L” and CS2 = “H”), the serial data input (SI) and the serial clock input (SCL) can be received. The serial data is read from the serial data input pin in the rising edge of the serial clocks D7, D6 through D0, in this order. This data is converted to 8 bits of parallel data in the rising edge of eighth serial clock for processing.

The A0 input is used to determine whether or not the serial data input is display data, and when A0 = “L” then the data is command data. The A0 input is read and used for detection of every 8th rising edge of the serial clock after the chip becomes active. Figure 1 is the serial interface signal chart.

Figure 1



Note:
1. When the chip is not active, the shift registers and the counters are reset to their initial states.
2. Reading is not possible while in serial interface mode.
3. Caution is required on the SCL signal when it comes to line-end reflections and external noise. We recommend that the operation can be rechecked on the actual equipment.

Chip Select Inputs

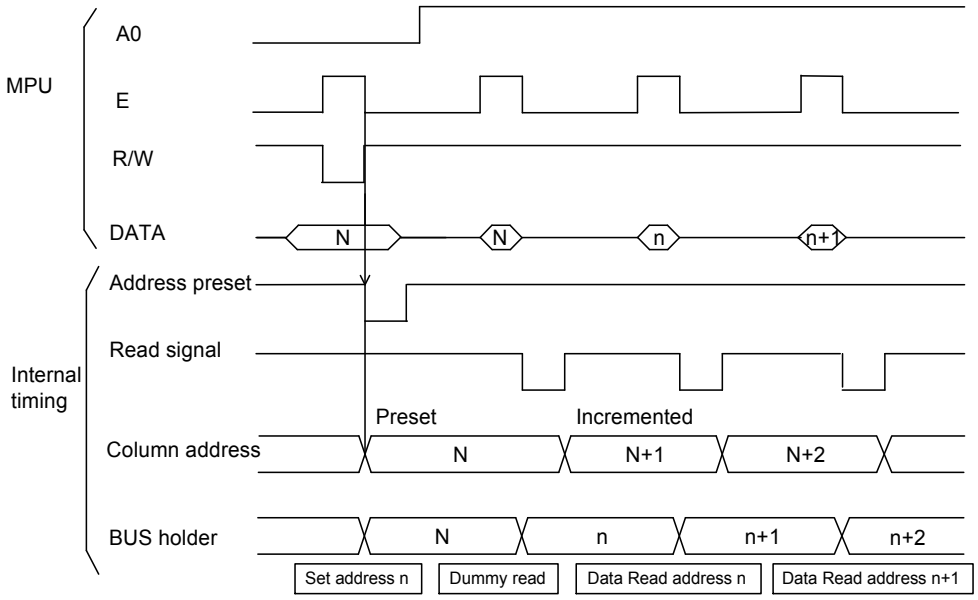
The NT7538 has two chip-select pads. /CS1 and CS2 can interface to a microprocessor when /CS1 is low and CS2 is high. When these pads are set to any other combination. D0 to D7 are high impedance and A0, E and R/W inputs are disabled. When serial input interface is selected, the shift register and counter are reset.

Access to Display Data RAM and Internal Registers

The NT7538 can perform a series of pipeline processing between LSI’s using the bus holder of the internal data bus in order to match the operating frequency of display RAM and internal registers with the microprocessor. For example, the microprocessor reads data from display RAM in the first read (dummy) cycle, stores it in the bus holder, and outputs it onto the system bus in the next data read cycle. Also, the microprocessor temporarily stores display data in the bus holder, and stores it in display RAM until the next data write cycle starts.

When viewed from the microprocessor, the NT7538 access speed greatly depends on the cycle time rather than access time to the display RAM (t_{ACC}). This view shows that the data transfer speed to / from the microprocessor can increase. If the cycle time is inappropriate, the microprocessor can insert the NOP instruction that is equivalent to the wait cycle setup. However, there is a restriction in the display RAM read sequence. When an address is set, the specified address data is NOT output at the immediately following read instruction. The address data is output during the second data read. A single dummy read must be inserted after address setup and after the write cycle (refer to Figure 2).

Figure 2



Busy Flag

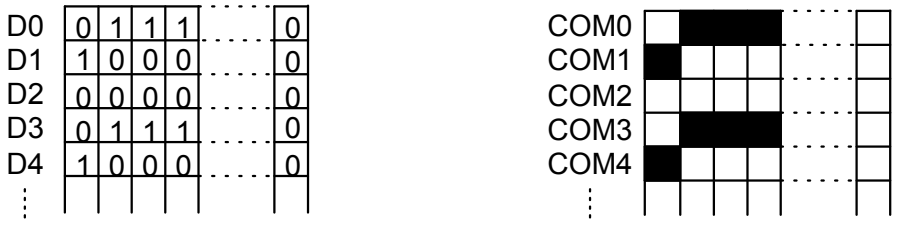
When the busy flag is “1” it indicates that the NT7538 chip is running internal processes, and at this time no command aside from a status read will be received. The busy flag is outputted to D7 pad with the read instruction. If the cycle time (t_{CYC}) is maintained, it is not necessary to check for this flag before each command. This makes vast improvements in MPU processing capabilities possible.

Display Data RAM

The display data RAM is RAM that stores the dot data for the display. It has a 65 (8 page * 8 bit+1)*132 bit structure. It is possible to access the desired bit by specifying the page address and the column address. Because, as is shown in Figure 3, the D7 to D0 display data from the MPU corresponds to the liquid crystal display common direction, there are few constraints at the time of display common direction, and there are few constraints at the time of display data transfer when multiple NT7538 chips are used, thus display structures can be created easily with a high degree of freedom.

Moreover, reading from and writing to the display RAM from the MPU side is performed through the I/O buffer, which is an independent operation from signal reading for the liquid crystal driver. Consequently, even if the display data RAM is accessed asynchronously during the liquid crystal display, it will not cause adverse effects on the display (such as flickering).

Figure 3



Display data RAM　　Display on LCD

The Page Address Circuit

As shown in Figure 4, page address of the display data RAM is specified through the Page Address Set Command. The page address must be specified again when changing pages to perform access. Page address8 (D3, D2, D1, D0 = 1, 0, 0, 0,) is the page for the RAM region used; only display data D0 is used.

The Column Address

As shown in Figure 4, the display data RAM column address is specified by the Column Address Set command. The specified column address is incremented (+1) with each display data read / write command. This allows the MPU display data to be accessed continuously. Moreover, the incrimination of column addresses stops with 83H, because the column address is independent of the page address. Thus, when moving, for example, from page 0 column 83H to page 1 column 00H, it is necessary to specify both the page address and the column address.

Furthermore, as is shown in Table 4, the ADC command (segment driver direction select command) can be used to reverse the relationship between the display data RAM column address and the segment output. Because of this, the constraints on the IC layout when the LCD module is assembled can be minimized.

Table 4

SEG Output	SEG0		SEG131
ADC "0"	0 (H)→	Column Address	→83 (H)
(ADC) "1"	83 (H)←	Column Address	←0 (H)

The Line Address Circuit

The line address circuit, as shown in Table 4, specifies the line address relating to the COM output when the contents of the display data RAM are displayed. Using the display start line address set command, what is normally the top line of the display can be specified. This is the COM0 output when the common output mode is normal and the COM63 output for NT7538, when the common output mode is reversed. The display area is a 65-line area for the NT7538 from the display start line address. If the line addresses are changed dynamically using the display start line address set command, screen scrolling, page swapping, etc. can be performed.

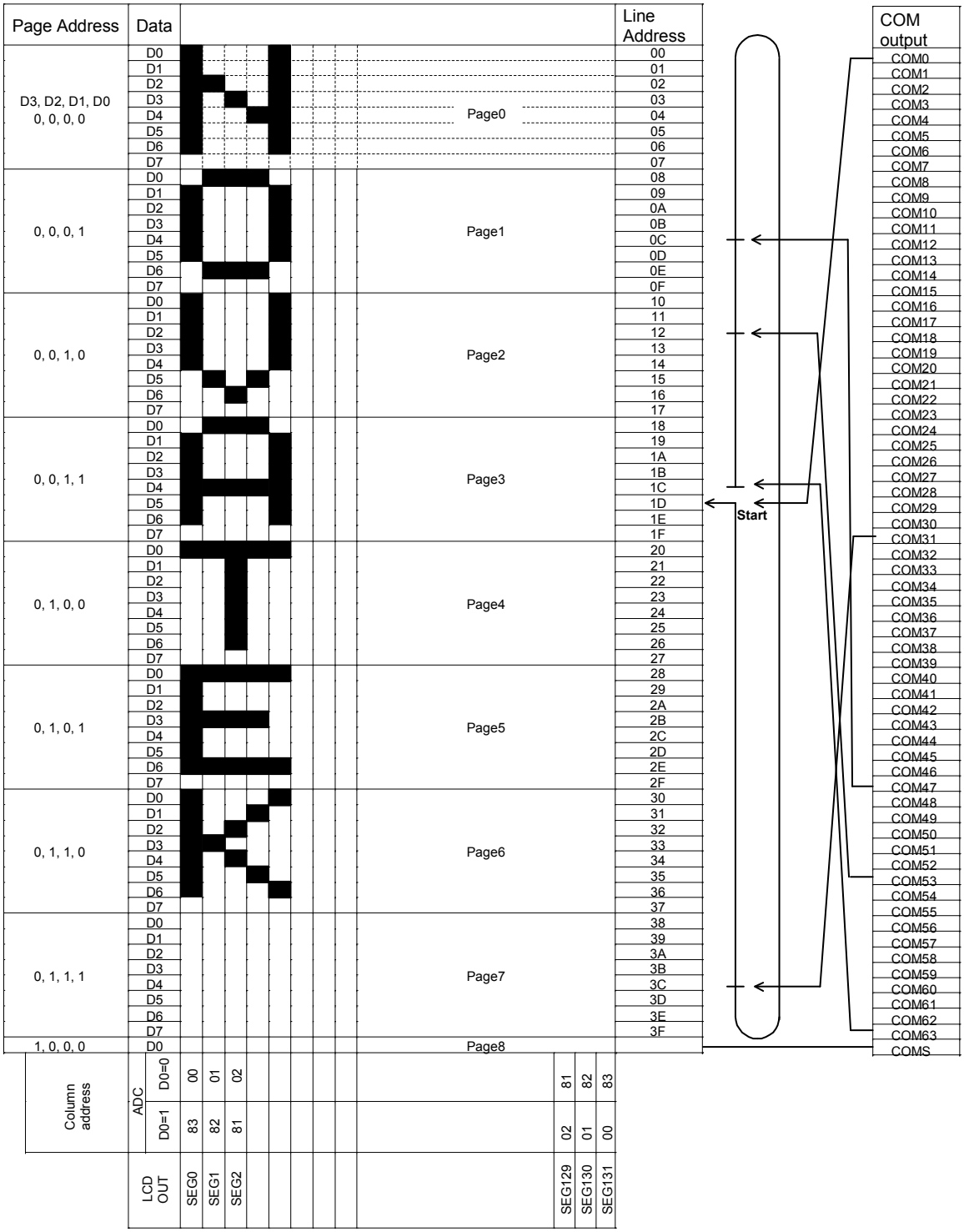
The Display Data Latch Circuit

The display data latch circuit is a latch that temporarily stores the display data that is output to the liquid crystal driver circuit from the display data RAM. Because the display normal/reverse status, display ON/OFF status, and display all points ON/OFF commands control only the data within the latch, they do not change the data within the display data RAM itself.

The Oscillator Circuit

This is a CR-type oscillator that produces the display clock. The oscillator circuit is only enabled when M/S = "H" and CLS = "H". When CLS = "L" the oscillation stops, and the display clock is input through the CL terminal.

Figure 4. Relationship between display data RAM and address. (if initial display line is 1DH)

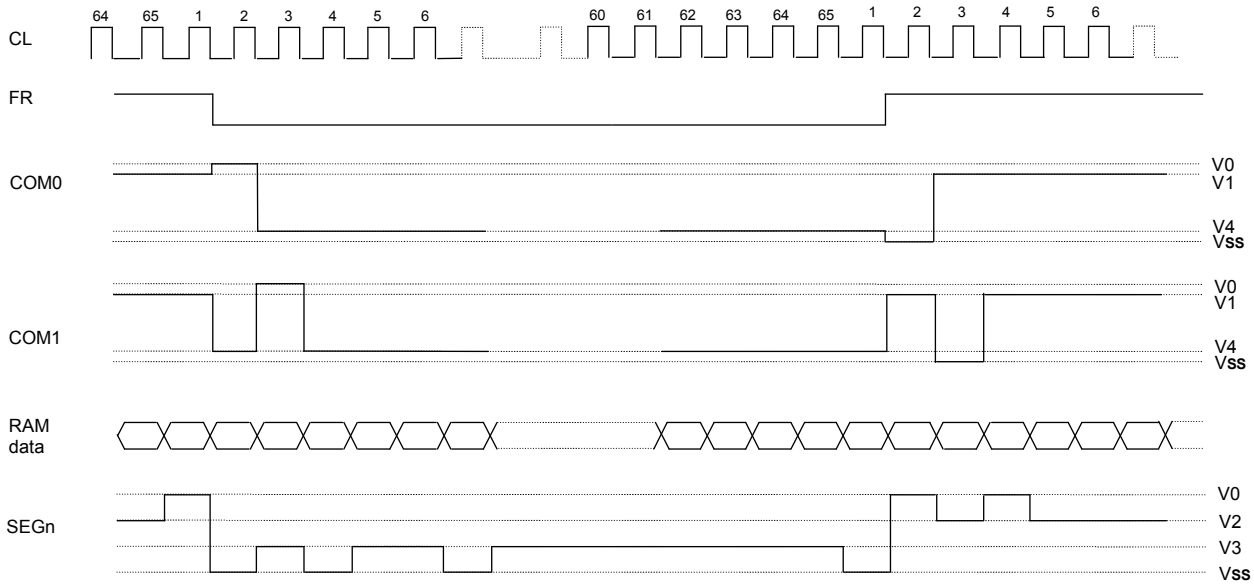


Display Timing Generator Circuit

The display timing generator circuit generates the timing signal to the line address circuit and the display data latch circuit using the display clock. The display data is latched into the display data latch circuit synchronized with the display clock, and is output to the data driver output terminal. Reading to the display data liquid crystal driver circuits is completely independent of access to the display data RAM by the MPU. Consequently, even if the display data RAM is accessed asynchronously during liquid crystal display, there is absolutely no adverse effect (such as flickering) on the display.

Moreover, the display timing generator circuit generates the common timing and the liquid crystal alternating current signal (FR) from the display clock. It generates a drive waveform using a 2 frames alternating current drive method, as shown in Figure 5, for the liquid crystal drive circuit.

Figure 5



When multiple NT7538 chips are used, the slave chip must be supplied with the display timing signals (FR, CL, /DOF) from the master chip. Table 5 shows the status of the FR, CL, and /DOF signals.

Table 5

Operating Mode		FR	CL	/DOF
Master (M/S = “H”)	The internal display oscillator is enabled (CLS = “H”)	Output	Output	Output
	The internal display oscillator is disabled (CLS = “L”)	Output	Input	Output
Slave (M/S = “L”)	The internal display oscillator is disabled (CLS = “H”)	Input	Input	Input
	The internal display oscillator is disabled (CLS = “L”)	Input	Input	Input

Table 6 shows the relationship between oscillation frequency and frame frequency. fOSC can be selected as 31.4K or 26.3KHz by using Oscilliation Frequency Select command.

Table 6

Duty	Item	fCL	fFR
1/65	On-chip oscillator is used	fOSC/6	fCL/(2 x 65)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 65)
1/49	On-chip oscillator is used	fOSC/8	fCL/(2 x 49)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 49)
1/33	On-chip oscillator is used	fOSC/12	fCL/(2 x 33)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 33)
1/17	On-chip oscillator is used	fOSC/22	fCL/(2 x 17)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 17)
1/9	On-chip oscillator is used	fOSC/44	fCL/(2 x 9)
	On-chip oscillator is not used	External input fCL	fCL/(2 x 9)

Common Output Control Circuit

This circuit controls the relationship between the number of common output and specified duty ratio. Common output mode select instruction specifies the scanning direction of the common output pads.

Table 7

Duty	Status	Common output pads							
		COM [0-15]	COM [16-23]	COM [24-26]	COM [27-36]	COM [37-39]	COM [40-47]	COM [48-63]	COMS
1/33	Normal	COM[0-15]	NC					COM[16-31]	COMS
	Reverse	COM[31-16]	NC					COM[15-0]	
1/49	Normal	COM[0-23]		NC			COM[24-47]		COMS
	Reverse	COM[47-24]		NC			COM[23-0]		
1/65	Normal	COM[0-63]							COMS
	Reverse	COM[63-0]							

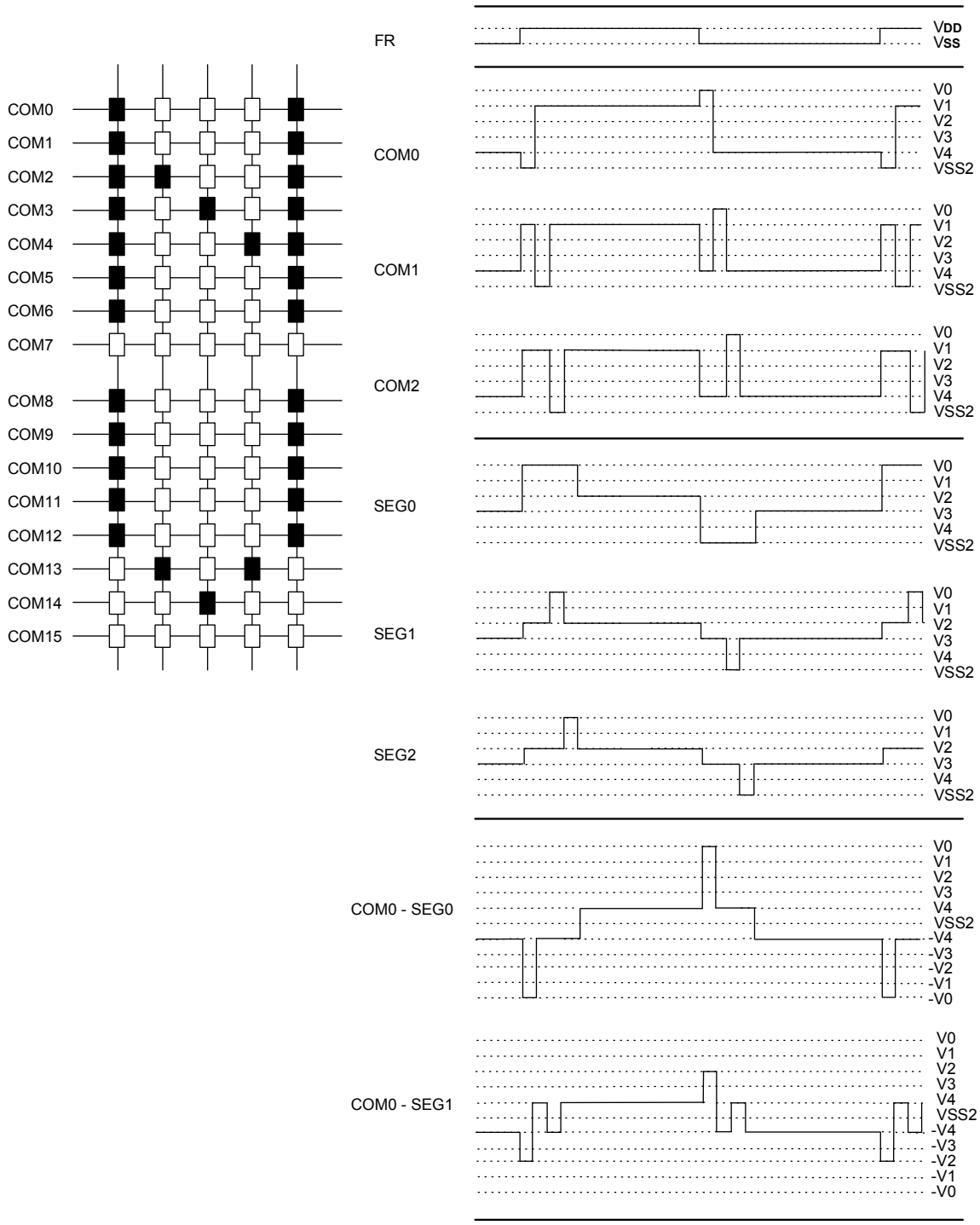
The combination of the display data, the COM scanning signals, and the FR signal produces the liquid crystal drive voltage output. Figure 6 shows example of the SEG and COM output waveform.

Configuration Setting

The NT7538 has two optional configurations, configured by DUTY0, DUTY1.

DUTY1, DUTY0	Common	Segment	V1	V2	V3	V4
1, 0 or 1, 1	65	132	8/9V0, 6/7V0	7/9V0, 5/7V0	2/9V0, 2/7 V0	1/9V0, 1/7V0
0, 1	49	132	7/8V0, 5/6V0	6/8V0, 4/6V0	2/8V0, 2/6 V0	1/8V0, 1/6V0
0, 0	33	132	5/6V0, 4/5V0	4/6V0, 3/5V0	2/6 V0, 2/5V0	1/6V0, 1/5V0

Figure 6


COM0
COM1
COM2
COM3
COM4
COM5
COM6
COM7
COM8
COM9
COM10
COM11
COM12
COM13
COM14
COM15
FR
VDD
VSS
COM0
COM1
COM2
SEG0
SEG1
SEG2
COM0 - SEG0
COM0 - SEG1
V0
V1
V2
V3
V4
VSS2
-V4
-V3
-V2
-V1
-V0

The Power Supply Circuit

The power supply circuits are low-power consumption power supply circuits that generate the voltage levels required for the liquid crystal drivers. They comprise Booster circuits, voltage regulator circuits, and voltage follower circuits. They are only enabled in master operation.

The power supply circuits can turn the booster circuits, the voltage regulator circuits, and the voltage follower circuits ON or OFF independently through the use of the Power Control Set command. Consequently, it is possible to make an external power supply and the internal power supply function somewhat in parallel. Table 8 shows the Power Control Set Command 3-bit data control functions, and Table 9 shows reference combinations.

Table 8

Item	Status	
	"1"	"0"
D2 Voltage Booster (V/B) circuit control bit	ON	OFF
D1 Voltage regulator (V/R) circuit control bit	ON	OFF
D0 Voltage follower (V/F) circuit control bit	ON	OFF

Table 9

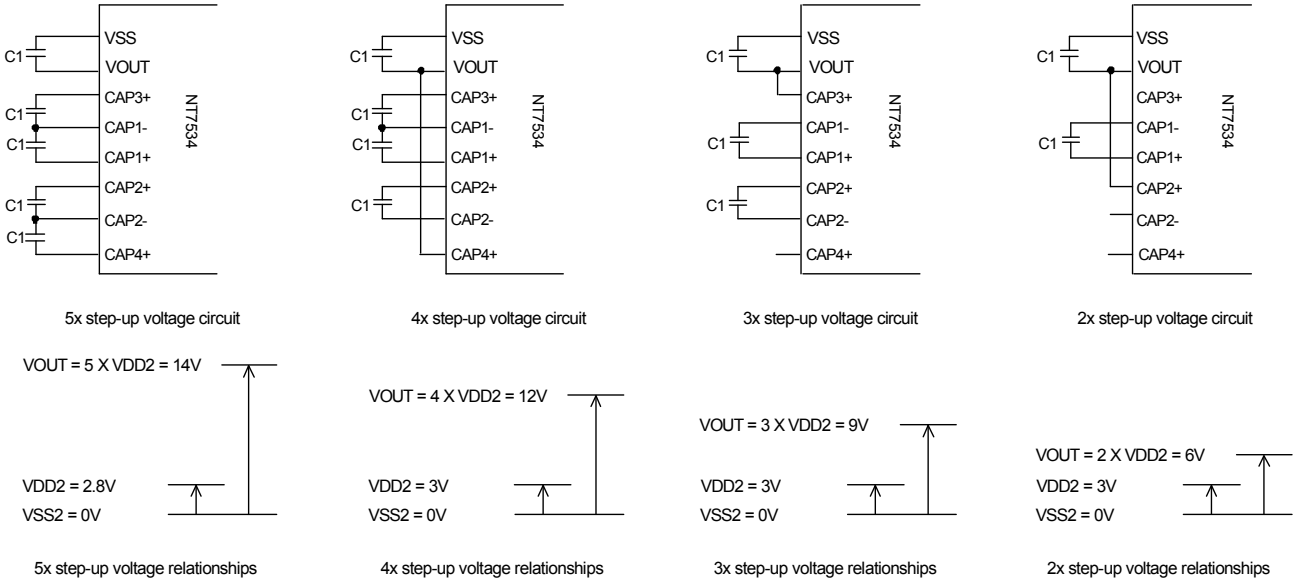
Use Settings	D2	D1	D0	V/B Circuit	V/R circuit	V/F circuit	External voltage input	Step-up voltage system terminal
Only the internal power supply is used	1	1	1	ON	ON	ON	VDD2	Used
Only the V/R circuit and the V/F circuit are used	0	1	1	OFF	ON	ON	VOUT, VDD2	Open
Only the V/F circuit is used	0	0	1	OFF	OFF	ON	V0, VDD2	Open
Only the external power supply is used	0	0	0	OFF	OFF	OFF	V0 to V4	Open

*The "Step-up system terminals" refer CAP1+, CAP1-, CAP2+, CAP2-, CAP3+ and CAP4+.
*While other combinations, not shown above, are also possible, these combinations are not recommended because they have no practical use.

The Step-up Voltage Circuits

Using the step-up voltage circuits within the NT7538 chips it is possible to product 5X, 4X, 3X, 2X step-ups of the VDD2-VSS2 voltage levels.

Figure 7



The Voltage Regulator Circuit

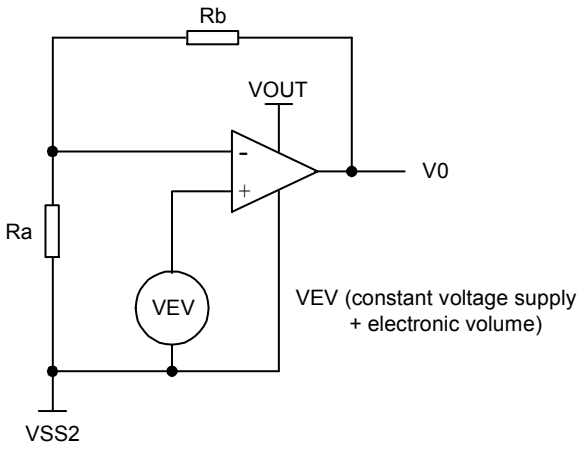
The step-up voltage generated at VOUT outputs the liquid crystal driver voltage V0 through the voltage regulator circuit. Because the NT7538 chips have an internal high-accuracy fixed voltage power supply with a 64-level electronic volume function and internal resistors for the V0 voltage regulator, systems can be constructed without having to include high-accuracy voltage regulator circuit components.

Moreover, NT7538 has thermal gradients: approximately –0.05%/°C.

When the V0 Voltage Regulator Internal Resistors Are Used

Through the use of the V0 voltage regulator internal resistors and the electronic volume function the liquid crystal power supply voltage V0 can be controlled by commands alone (without adding any external resistors), making it possible to adjust the liquid crystal display brightness. The V0 voltage can be calculated using equation A-1 over the range where V0 < VOUT.

$$V0 = (1+\frac{Rb}{Ra}) \times VEV = (1+\frac{Rb}{Ra}) \times (1-\frac{63-\alpha}{162}) \times VREG \qquad \text{(Equation A-1)}$$



VREG is the IC internal fixed voltage supply, and its voltage at Ta = 25°C is as shown in Table 10.

Table 10

Equipment Type	Thermal Gradient	Units	VREG
Internal Power Supply	-0.05	%/°C	1.4

α is set to 1 level of 64 possible levels by the electronic volume function depending on the data set in the 6-bit electronic volume register. Table 11 shows the value for α depending on the electronic volume register settings. Rb/Ra is the V0 voltage regulator internal resistor ratio, and can be set to 8 different levels through the V0 voltage regulator internal resistor ratio set command. The (1+Rb/Ra) ratio assumes the values shown in Table 12 depending on the 3-bit data settings in the V0 voltage regulator internal resistor ratio register.

Table 11

D5	D4	D3	D2	D1	D0	α	V0
0	0	0	0	0	0	0	Minimum
0	0	0	0	0	1	1	:
0	0	0	0	1	0	2	:
		:			:	:	:
1	0	0	0	0	0	32	(default)
		:			:	:	:
1	1	1	1	1	0	62	:
1	1	1	1	1	1	63	Maximum

V0 voltage regulator internal resistance ratio register value and (1+ Rb/Ra) ratio (Reference value)

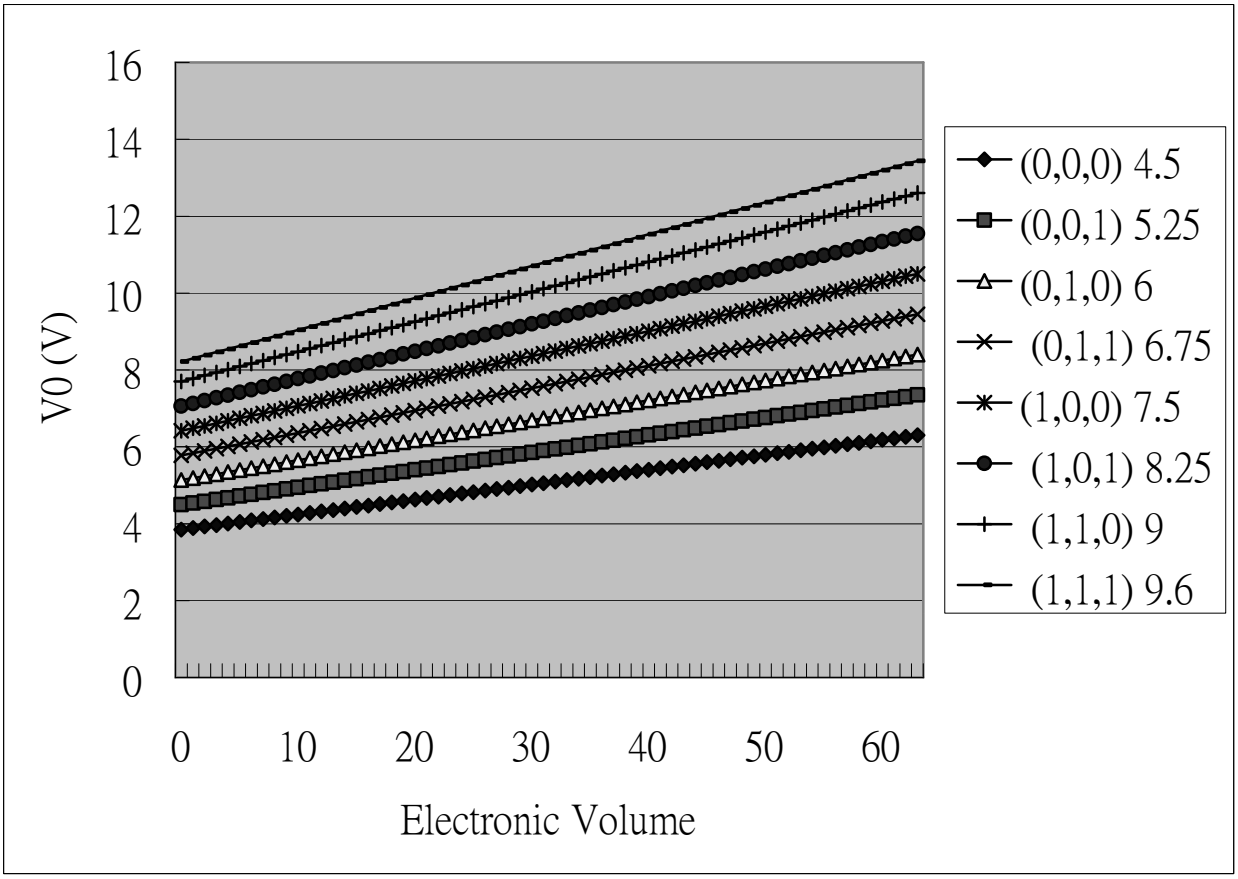
Table 12

Register			Equipment Type by Thermal Gradient [Units:%/°C]
D2	D1	D0	-0.05
0	0	0	4.50
0	0	1	5.25
0	1	0	6.00
0	1	1	6.75
1	0	0	7.50 (default)
1	0	1	8.25
1	1	0	9.00
1	1	1	9.60

The V0 voltage as a function of the V0 voltage regulator internal resistor ratio register and the electronic volumn register.

Note: When selecting external Rb/Ra resistors, Ra+Rb shoud be greater than 1.5MΩ.

Figure 8. The Contrast Curve of V0 Voltage with internal resistors



Setup example: When selecting Ta=25°C and V0=7V for a NT7538 model on which the temperture compemsation is internal, using the equation A-1, the following setup is enable.

Table 13

Contents	Register					
	D5	D4	D3	D2	D1	D0
For V0 voltage regulator	-	-	-	0	1	0
Electronic Volume	1	0	0	1	0	1

- When the V0 voltage regulator internal resistors or the electronic volume function is used, it is necessary to at least set the voltage regulator circuit and the voltage follower circuit to an operating mode using the power control set commands. Moreover, it is necessary to provide a voltage from VOUT when the Booster circuit is OFF.
- The VR terminal is enabled only when the V0 voltage regulator internal resistors are not used (i.e. the IRS terminal = “L”). When the V0 voltage regulator internal resistors are used (i.e. when the IRS ternimal = “H”), then the VR terminal is left open.
- Because the input impedance of the VR terminal is high, it is necessary to take into consideration short leads, shield cables,etc. to handle noise.

The Liquid Crystal Voltage Generator Circuit

The V0 voltage is produced by a resistive voltage divider within the IC, and can be produced at the V1, V2, V3, and V4 voltage levels required for liquid crystal driving. Moreover, when the voltage follower changes the impedance, it provides V1, V2, V3, and V4 to the liquid crystal drive circuit. 1/9 bias or 1/7 bias for NT7538 can be selected when the duty is 1/65.

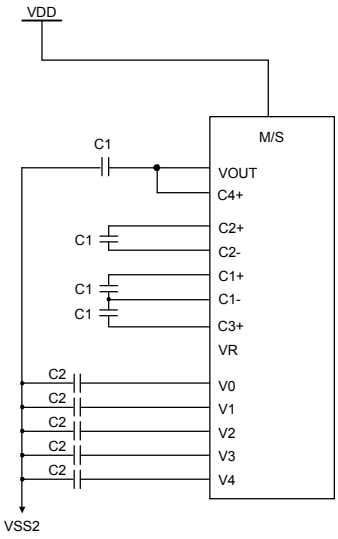
High Power Mode

The power supply circuit equipped in the NT7538 chips has very low power consumption (normal mode: /HPM="H"). However for LCDs or panels with large loads, this low-power power supply may cause display quality to degrade. When this occurs, setting the /HPM terminal to "L" (high power mode) can improve the quality of the display. We recommend that the display be checked on actual equipment to determine whether or not to use this mode.

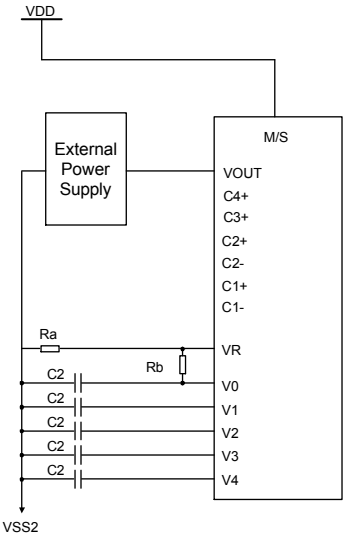
Moreover, if the improvement to the display is inadequate even after the high power mode has been set, then it is necessary to add a liquid crystal drive power supply externally.

Reference Power Supply Circuit for Driving LCD Panel

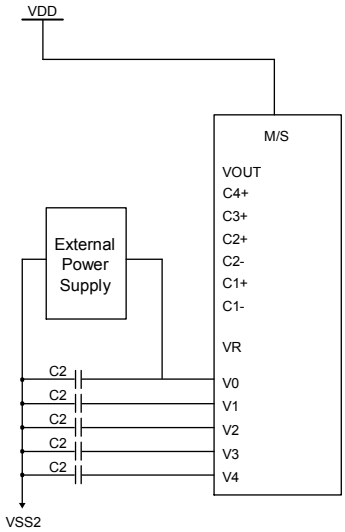
-When using all LCD power circuits
(Voltage booster, regulator and follower)
(In case of 4X boosting circuit and internal regulator resistors, IRS=1)



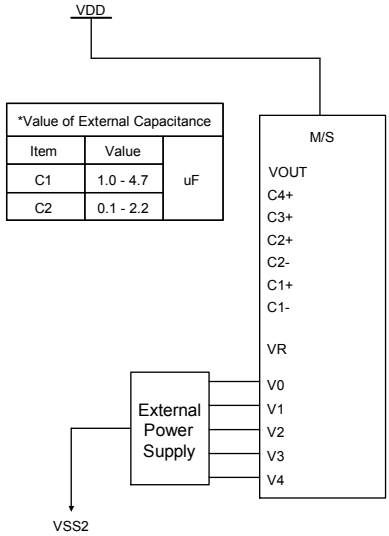
--When not using voltage booster circuits
(In case of external regulator resistors, IRS=0)



-When only using voltage follower



-When not using internal LCD power supply circuits



Reset Circuit

When the /RES input falls to “L”, these LSIs reenter their default state. The default settings are shown below:

1. Display OFF
2. Normal display
3. ADC select: Normal display (ADC command D0 = “L”)
4. Power control register (D2, D1, D0) = (0, 0, 0,)
5. Register data clear in serial interface
6. LCD power supply bias ratio 1/9 (1/65 duty), 1/8 (1/49 duty), 1/6 (1/33 duty)
7. Read modify write OFF
8. Static indicator: OFF
   Static indicator register: (D1, D2) = (0, 0)
9. Display start line register set at first line
10. Column address counter set at address 0
11. Page address register set at page 0
12. Common output status normal
13. V0 voltage regulator internal power supply ratio set mode clear:
    V0 voltage regulator internal resistor ratio register: (D2, D1, D0) = (1, 0, 0)
14. Electronic volume register set mode clear
    Electronic volume register: (D5, D4, D3, D2, D1, D0) = (1, 0, 0, 0, 0, 0,)
15. Test mode clear
16. Oscillation frequency 31.4 KHz
17. Normal display mode and frame inversion status (partial display and N-Line inversion release)
18. N-Line inversion register: (D4, D3, D2, D1, D0) = (0, 1, 1, 0, 0), 13-Line inversion
19. Partial start line register: (D5, D4, D3, D2, D1, D0) = (0, 0, 0, 0, 0, 0), the first line
20. DC/DC clock division register: (D3, D2, D1, D0) = (0, 0, 1, 1), fOSC/6
21. Output condition of COM, SEG
    COM: VSS
    SEG: VSS

On the other hand, when the reset command is used, only default settings 7 to 15 above are put into effect.

The MPU interface (Reference Example)”, the /RES terminal is connected to the MPU reset terminal, making the chip reinitialize simultaneously with the MPU. At the time of power up, it is necessary to reinitialize using the /RES terminal. Moreover, when the control signal from the MPU is in a high impedance state, there may be an overcurrent condition; therefore, take measures to prevent the input terminal from entering a high impedance state.

In the NT7538, if the internal liquid crystal power supply circuit is not used, user has to supply the external liquid crystal power after the procedure of RESET has been finished (please refer to the timing chart of Reset). During the period of external liquid crystal power supply being supplied, the /RES must be kept “H”.

Even though the oscillator circuit operates while the /RES terminal is “L,” the display timing generator circuit is stopped, the FR and FRS terminals are fixed to “H”, the /DOF and CL pins are fixed to “L” only when the intermal oscillator circuit is used. There is no influence on the D0 to D7 terminals..

Commands

The NT7538 uses a combination of A0, /RD (E) and /WR (R/W) signals to identify data bus signals. As the chip analyzes and executes each command using internal timing clock only regardless of external clock, its processing speed is very high and its busy check is usually not required. The 8080 series microprocessor interface enters a read status when a low pulse is input to the /RD pad and a write status when a low pulse is input to the /WR pad. The 6800 series microprocessor interface enters a read status when a high pulse is input to the R/W pad and a write status when a low pulse is input to this pad. When a high pulse is input to the E pad, the command is activated. (For timing, see AC Characteristics.). Accordingly, in the command explanation and command table, /RD (E) becomes 1(high) when the 6800 series microprocessor interface reads status of display data. This is the only different point from the 8080 series microprocessor interface.

Taking the 8080 series microprocessor interface as an example, commands are explained below. When the serial interface is selected, input data starting from D7 in sequence.

1. Display ON/OFF

   Alternatively turns the display on and off.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	1	1	AFh	Display ON
										0	AEh	Display OFF

   When the display OFF command is executed when in the display all points ON mode, power save mode is entered. See the section on the power saver for details.

2. Display Start Line Set

   Specifies line address (refer to Figure 6) to determine the initial display line, or COM0. The RAM display data becomes the top line of LCD screen. The higher number of lines in ascending order, corresponding to the duty cycle follows it. When this command changes the line address, smooth scrolling or a page change takes place.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	1	A5	A4	A3	A2	A1	A0	40h to 7Fh

A5	A4	A3	A2	A1	A0	Line address
0	0	0	0	0	0	0
0	0	0	0	0	1	1
0	0	0	0	1	0	2
			:			:
1	1	1	1	1	0	62
1	1	1	1	1	1	63

3. Page Address Set

Specifies page address to load display RAM data to page address register. Any RAM data bit can be accessed when its page address and column address are specified. The display remains unchanged even when the page address is changed. Page address 8 is the display RAM area dedicated to the indicator, and only D0 is valid for data change.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	1	1	A3	A2	A1	A0	B0h to B8h

A3	A2	A1	A0	Page address
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
	:			:
0	1	1	1	7
1	0	0	0	8

4. Column Address Set

Specifies column address of display RAM. Divide the column address into 4 higher bits and 4 lower bits. Set each of them succession. When the microprocessor repeats to access the display RAM, the column address counter is incremental by during each access until address 132 is accessed. The page address is not changed during this time.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	
0	1	0	0	0	0	1	A7	A6	A5	A4	10h to 18h	High nibble
						0	A3	A2	A1	A0	00h to 0Fh	Low nibble

A7	A6	A5	A4	A3	A2	A1	A0	Column address
0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1	1
0	0	0	1	0	1	1	0	2
				:				:
1	0	0	0	0	0	1	0	130
1	0	0	0	0	0	1	1	131

5. Read Status

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	/ADC	OFF/ON	RESET	0	0	0	0

BUSY: When high, the NT7538 is busy due to internal operation or reset. Any command is rejected until BUSY goes low. The busy check is not required if enough time is provided for each cycle.

/ADC: Indicates the relationship between RAM column address and segment drivers. When low, the display is reversed and column address “131-n” corresponds to segment driver n. when high, the display is normal and column address corresponds to segment driver n.

OFF/ON: Indicates whether the display is on or off. When low, the display turns on. When high, the display turns off. This is the opposite of Display ON/OFF command.

RESET: Indicates the initialization is in progress by /RES signal or by reset command. When low, the display is on. When high, the chip is being reset.

6. Write Display Data

Write 8-bit data in display RAM. As the column address automatically increments by 1 after each write, the microprocessor can continue to write data of multiple words.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write Data							

7. Read Display Data

Reads 8-bit data from display RAM area specified by column address and page address. As the column address automatically increments by 1 after each write, the microprocessor can continue to read data of multiple words. A single dummy read is required immediately after column address setup. Refer to the display RAM section of FUNCTIONAL DESCRIPTION for details. Note that no display data can be read via the serial interface.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read Data							

8. ADC Select

Changes the relationship between RAM column address and segment driver. The order of segment driver output pads could be reversed by software. This allows flexible IC layout during LCD module assembly. For details, refer to the column address section of Figure 4. When display data is written or read, the column address is incremented by 1 as shown in Figure 4.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	0	0	0	A0h	Normal
										1	A1h	Reverse

9. Normal/ Reverse Display

Reverses the Display ON/OFF status without rewriting the contents of the display data RAM.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	1	0	A6h	RAM Data “H” LCD ON voltage (normal)
										1	A7h	RAM Data “L” LCD ON voltage (reverse)

10. Entire Display ON

Forcibly turns the entire display on regardless of the contents of the display data RAM. At this time, the contents of the display data RAM are held. This command has priority over the Normal/Reverse Display command. When D is low, the normal display status is provided.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	0	1	0	0	A4h	Normal display mode
										1	A5h	Display all points ON

When D0 is high, the entire display ON status is provided. If the Entire Display ON command is executed in the display OFF status, the LCD panel enters Power save mode. Refer to the Power Save section for details.

11. LCD Bias Set

This command selects the voltage bias ratio required for the liquid crystal display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Duty		
												1/33	1/49	1/65
0	1	0	1	0	1	0	0	0	1	0	A2h	1/6 bias	1/8 bias	1/9 bias
										1	A3h	1/5 bias	1/6 bias	1/7 bias

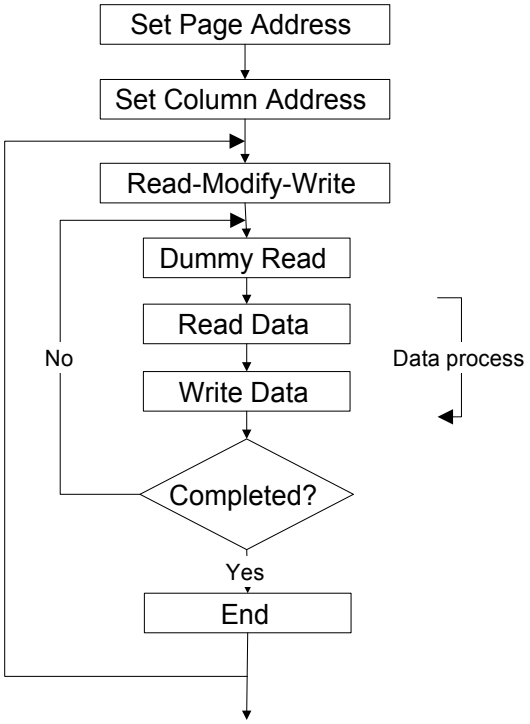
12. Read-Modify-Write

A pair of Read-Modify-Write and End commands must always be used. Once Read-Modify-Write is issued, column address is not incremental by Read Display Data command but incremental by Write Display Data command only. It continues until End command is issued. When the End is issued, column address returns to the address when Read-Modify-Write is issued. This can reduce the microprocessor load when data of a specific display area is repeatedly changed during cursor blinking or other events.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	0	0	E0h

Note: Any command except Read/Write Display Data and Column Address Set can be issued during Read-Modify-Write mode.

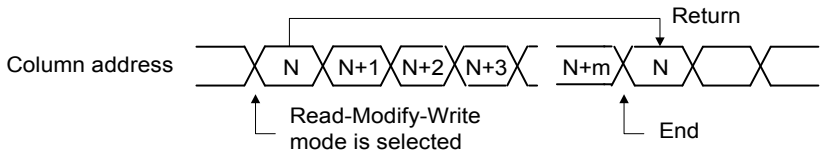
Cursor display sequence



13. End

Cancels Read-Modify-Write mode and returns column address to the original address (when Read-Modify-Write is issued)

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	1	1	1	0	EEh



14. Reset

This command resets the Display Start Line register, Column Address counter, Page Address register, and Common output mode register, the V0 voltage regulator internal resistor ratio register, the Electronic Volume register, the static indicator mode register, the read-modify-write mode register, and the test mode. The Reset command does not affect on the contents of display RAM. Refer to the Reset circuit section of Function Description.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	1	0	E2h

The Reset command cannot initialize LCD power supply. Only the Reset signal to the /RES pad can initialize the supplies.

15. Output Status Select Register

When D3 is high or low, the scan direction of the COM output pad is selectable. Refer to Output Status Selector Circuit in Function Description for details.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	0	0	0	*	*	*	C0h to C7h
							1				C8h to CFh

*: Invalid bit
D3 = 0: Normal (COM0 → COM63/47/31)
D3 = 1: Reverse (COM63/47/31 → COM0)

16. Power Control Set

Select one of eight power circuit functions using 3-bit register. An external power supply and part of on-chip power circuit can be used simultaneously. Refer to Power Supply Circuit section of FUNCTIONAL DESCRIPTION for details.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	0	0	1	0	1	A2	A1	A0	28h to 2Fh

When A0 goes low, voltage follower turns off. When A0 goes high, it turns on.
When A1 goes low, voltage regulator turns off. When A1 goes high, it turns on.
When A2 goes low, voltage booster turns off. When A2 goes high, it turns on.

17. V0 Voltage Regulator Internal Resistor Ratio Set

This command sets the V0 voltage regulator internal resistor ratio. For details, see explanation under “The Power Supply Circuits”.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Rb/Ra Ratio
0	1	0	0	0	1	0	0	0	0	0	20h	Small
								0	0	1	21h	
								0	1	0	22h	
									:		:	:
								1	1	0	26h	
								1	1	1	27h	Large

18. The Electronic Volume (Double Byte Command)

This command makes it possible to adjust the brightness of the liquid crystal display by controlling the liquid crystal drive voltage V0 through the output from the voltage regulator circuits of the internal liquid crystal power supply. It is a two-byte command used as a pair with the electronic volume mode set command and the electronic volume register set command, and both commands must be issued one after the other.

(1) The Electronic Volume Mode Set

When this command is input, the electronic volume register set command is enabled. Once the electronic volume mode has been set, no other command except for the electronic volume register command can be used. Once the electronic volume register set command has been used to set data into the register, then the electronic volume mode is released.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	0	0	1	81h

(2) Electronic Volume Register Set

By using this command to set six bits of data to the electronic volume register, the liquid crystal voltage V0 assumes one of the 64 voltage levels. When this command is input, the electronic volume mode is released after the electronic volume register has been set.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	V0
0	1	0	*	*	0	0	0	0	0	1	XX	Small
					0	0	0	0	1	0	XX	
									:		:	:
					1	1	1	1	1	0	XX	
					1	1	1	1	1	1	XX	Large

When the electronic volume function is not used, set D5 - D0 to 100000.

19. Static Indicator (Double Byte Command)

This command controls the static drive system indicator display. The static indicator display is controlled by this command only, and is independent of other display control commands.

This is used when one of the static indicator liquid crystal drive electrodes is connected to the FR terminal, and the other is connected to the FRS terminal. A different pattern is recommended for the static indicator electrodes than for the dynamic drive electrodes. If the pattern is too close, it can result in deterioration of the liquid crystal and of the electrodes.

The static indicator ON command is a double bytes command paired with the static indicator register set command, and thus command must be executed one after the other. (The static indicator OFF command is a single byte command)

(1) Static Indicator ON/OFF

When the static indicator ON command is entered, the static indicator register set command is enabled. Once the static indicator ON command has been entered, no other command aside from the static indicator register set command can be used. This mode is cleared when data is set in the register by the static indicator register set command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Setting
0	1	0	1	0	1	0	1	1	0	0	ACh	Static Indicator OFF
										1	ADh	Static Indicator ON

(2) Static Indicator Register Set

This command sets two bits of data into the static indicator register and used to set the static indicator into a blinking mode.

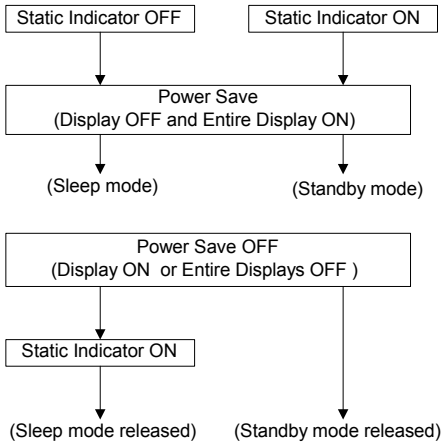
A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Indicator Display Status
0	1	0	*	*	*	*	*	*	0	0	XX	OFF
									0	1	XX	ON (blinking at approximately 1 second intervals)
									1	0	XX	ON (blinking at approximately 0.5 second intervals)
									1	1	XX	ON (constantly on)

20. Power Save (Compound Command)

When all displays are turned on during display off, the Power Save command is issued to greatly reduce current consumption.

If the static indicator is off, the Power Save command makes the system enter sleep mode. If the static indicator is on, this command makes the system enter standby mode.

Release the Sleep mode using the both Power Save OFF command (Display ON command or Entire Display OFF command) and Set Indicator On command.



Sleep Mode

This mode stops every operation of the LCD display system, and can reduce current consumption nearly to a static current value if no access is made from the microprocessor. The internal status in the sleep mode is as follows:

(1) Stops the oscillator circuit and LCD power supply circuit.
(2) Stops the LCD driver and outputs the VSS level as the segment/common driver output.
(3) Holds the display data and operation mode provided before the start of the sleep mode.
(4) The MPU can access the built-in display data RAM.

Standby Mode

Stops the operation of the duty LCD displays system and turns on only the static drive system to reduce current consumption to the minimum level required for static drive. The ON operation of the static drive system indicates that the NT7538 is in standby mode. The internal status in the standby mode is as follows:

(1) Stops the LCD power supply circuit.
(2) Stops the LCD drive and outputs the VSS level as the segment / common driver output. However, the static drive system still operates.
(3) Holds the display data and operation mode provided before the start of the standby mode.
(4) The MPU can access the built-in display data RAM.

When the Reset command is issued in the standby mode, the sleep mode is set.

- When the LCD drive voltage level is given by an external resistive driver, the current of this resistor must be cut so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7538 to go to the sleep mode or standby mode.
- When an external power supply is used, likewise, the function of this external power supply must be stopped so that it may be fixed to floating or VSS level, prior to or concurrently with causing the NT7538 to go to the sleep mode or standby mode.

21. NOP

Non-Operation Command.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	0	1	1	E3h

22. Test Command

This is the dedicated IC chip test command. It must not be used for normal operation. If the Test command is issued inadvertently, set the /RES input to low or issue the Reset command to release the test mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	1	0	1	0	0	F0h to FFh

*: Invalid bit

Cautions: The NT7538 maintains an operation status specified by each command. However, the internal operation status may be changed by a high level of ambient noise. Users must consider how to suppress noise on the package and system or to prevent ambient noise insertion. To prevent a spike in noise, built-in software for periodical status refreshment is recommended. The test command can be inserted in an unexpected place. Therefore it is recommended to enter the test mode reset command F0h during the refresh sequence.

23. Oscillation Frequency Select

This command is to select the oscillation frequency of driver IC as below.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Oscillation Frequency
0	1	0	1	1	1	0	0	1	0	0	E4h	Typical 31.4 KHz
										1	E5h	Typical 26.3 KHz

24. Partial Display Mode Set

This command enables to select the display mode. When D0 is low, the IC is in normal display mode, the maximum display duty ratio is decided by pin connection of DUTY0 and DUTY1 and the command LCD Bias Set decides the LCD bias ratio. The IC enters into partial display mode when D0 is high, then the commands Partial Display Duty Set and Partial Display Bias Set decide the LCD display duty and bias ratios.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Display Mode
0	1	0	1	0	0	0	0	0	1	0	82h	Normal Display
										1	83h	Partial Display

25. Partial Display Duty and Bias Set

These two commands set the LCD display duty and bias ratios when the IC is in partial display mode. They are invalid when the IC is in normal display mode. When the partial display duty is set, the LCD bias for partial display is set simultaneous as below. The partial display duty will be kept at maximum duty (decided by pins DUTY0 and DUTY1) when setting duty is larger than maximum duty.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Duty	Scanning Line
0	1	0	0	0	1	1	0	0	0	0	30h	1/9 duty	Line [0:7], COMS
								0	0	1	31h	1/17 duty	Line [0:15], COMS
								0	1	0	32h	1/33 duty	Line [0:31], COMS
								0	1	1	33h	1/49 duty	Line [0:47], COMS
								1	0	0	34h	1/65 duty	Line [0:63], COMS
								1 1	0 1	1 *	35h 37h	Reserved	No effect

Using Partial Display Bias Set command to change the LCD bias in partial display mode.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	LCD Bias
0	1	0	0	0	1	1	1	0	0	0	38h	1/4
								0	0	1	39h	1/5
								0	1	0	3Ah	1/6
								0	1	1	3Bh	1/7
								1	0	0	3Ch	1/8
								1	0	1	3Dh	1/9
								1	1	0	3Eh	Reserved
								1	1	1	3Fh	Reserved

Note: The COM waveform of no display area is non-select waveform.

26. Partial Start Line Set (Double Byte Command)

This command makes it possible to set the partial start line for partial display. It is a two-byte command used as a pair and the Number of Start Line Set command must be issued after the Partial Start Line Set command.

(1) Partial Start Line Set

When this command is input, no other command except for the Number of Start Line Set command can be used.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	0	1	0	0	1	1	D3h

(2) Number of Start Line Set

By using this command to set six bits of data to the Partial Start Line register. Once the Number of the Start Line Set command has been used to set data into the register, then the partial start line will affect on the LCD display. The number of partial start line is always equal to zero when the partial start line is larger than maximum duty ratio (decided by pins DUTY0 and DUTY1).

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Partial Start Line
0	1	0	*	*	0	0	0	0	0	0	XX	0 line
					0	0	0	0	0	1	XX	1 line
					0	0	0	0	1	0	XX	2 line
								:			:	:
					1	1	1	1	1	0	XX	62 line
					1	1	1	1	1	1	XX	63 line

27. The N-Line Inversion (Double Byte Command)

This command makes it possible to adjust the number of scan lines for liquid crystal display inversion. It is a two-byte command used as a pair and the Number of Line Set command must be issued after the N-Line Inversion Set command.

(1) N-Line Inversion Set

When this command is input, no other command except for the Number of Line Set command can be used.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	1	0	1	85h

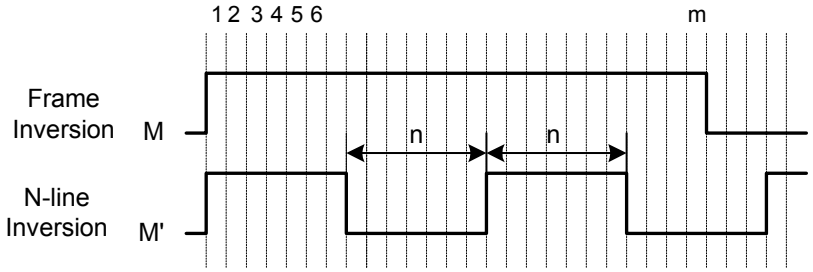
(2) Number of Line Set

By using this command to set five bits of data to the N-Line inversion register. Once the Number of Line Set command has been used to set the data into the register, then the N-Line inversion will affect on the LCD display.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Line Inversion
0	1	0	*	*	*	0	0	0	0	0	XX	1 line
						0	0	0	0	1	XX	2 line
								:			:	:
						1	1	1	1	1	XX	32 line

Note 1: The number of inversed scan line = register setting value + 1.

Note 2: When Partial Duty = 1/9 or 1/17, the N-line inversion function release and the LCD display scan line is back to frame inversion status.



28. Release N-Line Inversion

This command is used to exit the N-Line inversion function. The N-Line inversion function is released and the LCD display is set back to frame inversion status once this command is executed.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	0	0	0	0	1	0	0	84h

29. DC/DC Clock Frequency (Double Byte Command)

This command makes it possible to adjust the frequency for DC/DC clock. It is a two-byte command used as a pair and the DC/DC Frequency Division Set command must be issued after the DC/DC Clock Set command.

(1) DC/DC Clock Set

When this command is input, no other command except for the DC/DC Frequency Division Set command can be used.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex
0	1	0	1	1	1	0	0	1	1	0	E6h

(2) DC/DC Frequency Division Set

By using this command to set five bits of data to the frequency division register.

A0	E /RD	R/W /WR	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Division
0	1	0	*	*	*	*	0	0	0	0	XX	fOSC
							0	0	0	1	XX	fOSC/2
							0	0	1	0	XX	fOSC/4
							0	0	1	1	XX	fOSC/6 (default)
							0	1	0	0	XX	fOSC/8
							0	1	0	1	XX	fOSC/10
							0	1	1	0	XX	fOSC/12
							0	1	1	1	XX	fOSC/14
							1	0	0	0	XX	fOSC/16
							1	0	0	1	XX	fOSC/18
							1	0	1	0	XX	fOSC/20
							1	0	1	1	XX	fOSC/22
							1	1	0	0	XX	fOSC/24
							1	1	0	1	XX	fOSC/26
							1	1	1	0	XX	fOSC/28
							1	1	1	1	XX	fOSC/30

Table 14. Command Table

Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(1) Display OFF	0	1	0	1	0	1	0	1	1	1	0 1	AEh AFh	Turn on LCD panel when high, and turn off when low
(2) Display Start Line Set	0	1	0	0	1	Display Start Address						40h to 7Fh	Specifies RAM display line for COM0
(3) Page Address Set	0	1	0	1	0	1	1	Page Address				B0h to B8h	Set the display data RAM page in Page Address register
(4) Column Address Set	0	1	0	0	0	0	1	Higher Column Address				00h to 18h	Set 4 higher bits and 4 lower bits of column address of display data RAM in register
	0	1	0	0	0	0	0	Lower Column Address					
(5) Read Status	0	0	1	Status				0	0	0	0	XX	Reads the status information
(6) Write Display Data	1	1	0	Write Data								XX	Write data in display data RAM
(7) Read Display Data	1	0	1	Read Data								XX	Read data from display data RAM
(8) ADC Select	0	1	0	1	0	1	0	0	0	0	0 1	A0h A1h	Set the display data RAM address SEG output correspondence
(9) Normal/Reverse Display	0	1	0	1	0	1	0	0	1	1	0 1	A6h A7h	Normal indication when low, but full indication when high
(10)Entire Display ON/OFF	0	1	0	1	0	1	0	0	1	0	0 1	A4h A5h	Select normal display (0) or entire display on
(11)LCD Bias Set	0	1	0	1	0	1	0	0	0	1	0 1	A2h A3h	Sets LCD driving voltage bias ratio
(12)Read-Modify-Write	0	1	0	1	1	1	0	0	0	0	0	E0h	Increments column address counter during each write
(13)End	0	1	0	1	1	1	0	1	1	1	0	EEh	Releases the Read-Modify-Write
(14)Reset	0	1	0	1	1	1	0	0	0	1	0	E2h	Resets internal functions
(15)Common Output Mode Select	0	1	0	1	1	0	0	0 1	*	*	*	C0h to CFh	Select COM output scan direction *: invalid data
(16)Power Control Set	0	1	0	0	0	1	0	1	Operation Status			28h to 2Fh	Select the power circuit operation mode
(17)V0 Voltage Regulator Internal Resistor ratio Set	0	1	0	0	0	1	0	0	Resistor Ratio			20h to 27h	Select internal resistor ratio Rb/Ra mode
(18)Electronic Volume mode Set	0	1	0	1	0	0	0	0	0	0	1	81h	
Electronic Volume Register Set	0	1	0	*	*	Electronic Control Value						XX	Sets the V0 output voltage electronic volume register
(19)Set Static indicator ON/OFF	0	1	0	1	0	1	0	1	1	0	0 1	ACh ADh	Sets static indicator ON/OFF 0: OFF, 1: ON
Set Static Indicator Register	0	1	0	*	*	*	*	*	*	Mode		XX	Sets the flash mode
(20)Power Save	0	1	0	-	-	-	-	-	-	-	-	-	Compound command of Display OFF and Entire Display ON
(21)NOP	0	1	0	1	1	1	0	0	0	1	1	E3h	Command for non-operation

Command Table (continue)

Command	A0	/RD	/WR	Code									Function
				D7	D6	D5	D4	D3	D2	D1	D0	Hex	
(22)Oscillation Frequency Select	0	1	0	1	1	1	0	0	1	0	0 1	E4h E5h	Select the oscillation frequency
(23)Partial Display mode Set	0	1	0	1	0	0	0	0	0	1	0 1	82h 83h	Enter/Release the partial display mode
(24)Partial Display Duty Set	0	1	0	0	0	1	1	0	Duty Ratio			30h 37h	Sets the LCD duty ratio for partial display mode
(25)Partial Display Bias Set	0	1	0	0	0	1	1	1	Bias Ratio			38h 3Fh	Sets the LCD bias ratio for partial display mode
(26)Partial Start Line Set	0	1	0	1	1	0	1	0	0	1	1	D3h	Enter Partial Start Line Set
Partial Start Line Set	0	1	0	1	1	Partial Start Line						XX	Sets the LCD Number of partial display start line
(27)N-Line Inversion Set	0	1	0	1	0	0	0	0	1	0	1	85h	Enter N-Line inversion
Number of Line Set	0	1	0	*	*	*	Number of Line					XX	Sets the number of line used for N-Line inversion
(28)N-Line Inversion Release	0	1	0	1	0	0	0	0	1	0	0	84h	Exit N-Line Inversion
(29)DC/DC Clock Set	0	1	0	1	1	1	0	0	1	1	0	E6h	Set DC/DC Clock Frequency
DC/DC Clock Division Set	0	1	0	1	1	0	0	Clock Division				XX	Set the Division of DC/DC Clock Frequency
(30)Test Command	0	1	0	1	1	1	1	*	*	*	*	F1h to FFh	IC test command. Do not use!
(31)Test Mode Reset	0	1	0	1	1	1	1	0	0	0	0	F0h	Command of test mode reset

Note: Do not use any other command, or system malfunction may result.

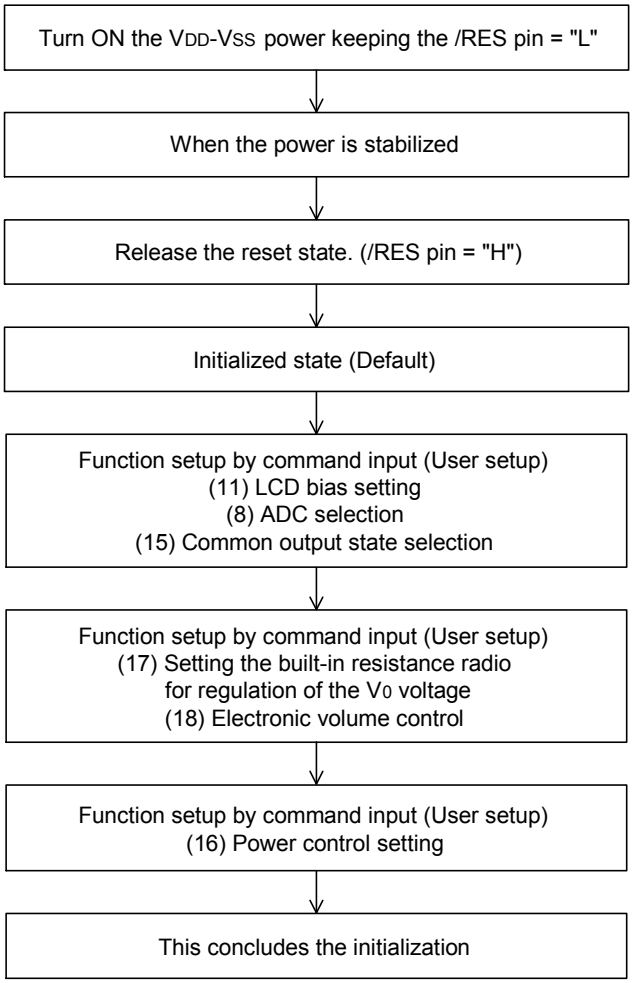
Command Description

Instruction Setup: Reference

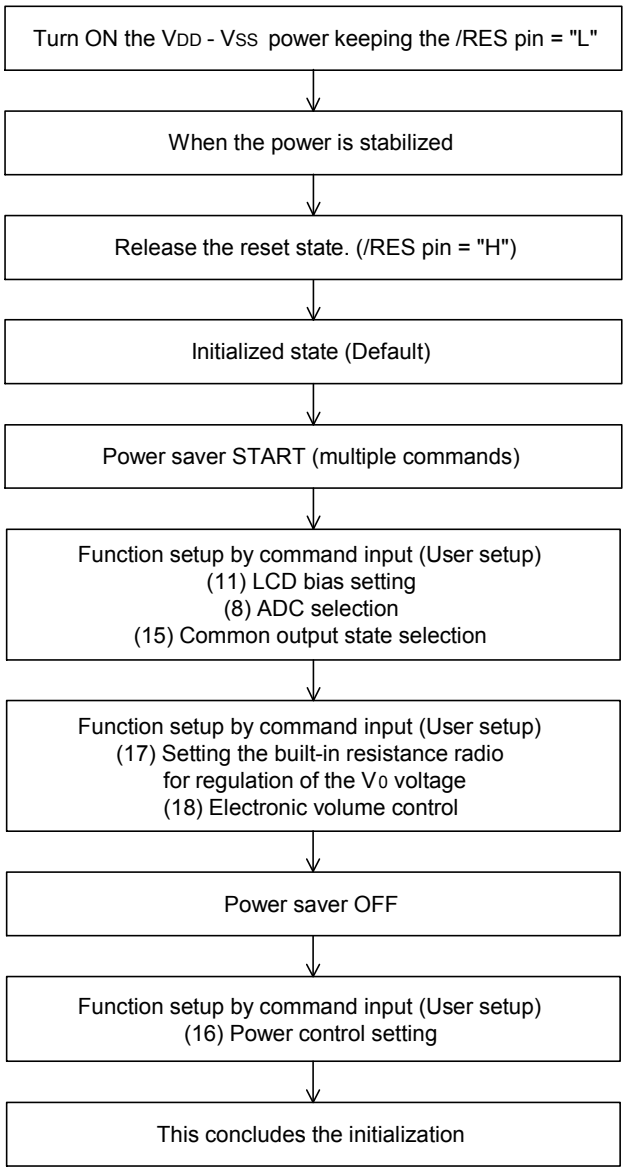
1. Initialization

   Note: With this IC, when the power is applied, LCD driving non-selective potentials V2 and V3 (SEG pin) and V1 and V4 (COM pin) are output through the LCD driving output pins SEG and COM. When electric charge is remaining in the smoothing capacitor connecting between the LCD driving voltage output pins (V0 - V4) and the VDD pin, the picture on the display may instantaneously become totally dark when the power is turned on. To avoid such failure, we recommend the following flow sequence when turning on the power.

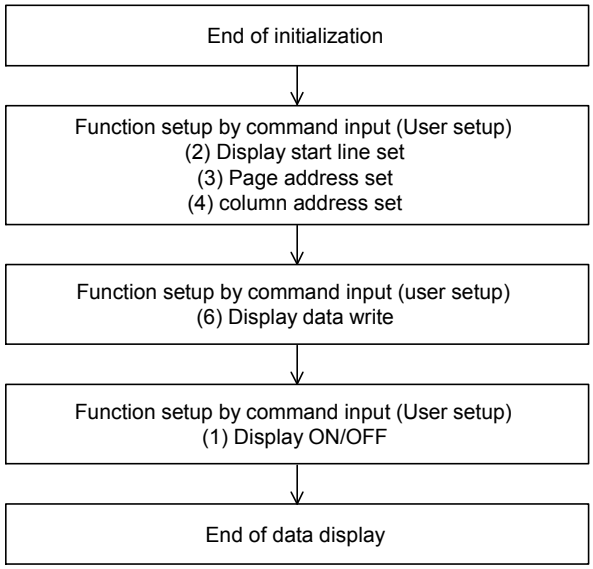
1.1. When the built-in power is being used immediately after turning on the power:



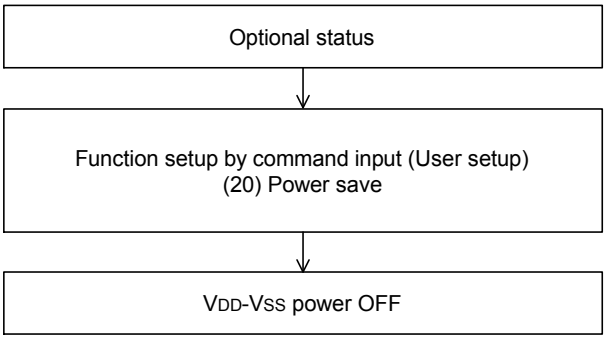
1.2. When the built-in power is not being used immediately after turning on the power



2. Data Display



3. Power OFF



Absolute Maximum Rating

DC Supply Voltage (VDD, VDD2, VDD3) ..... -0.3V to +4.0V
DC Supply Voltage (VOUT) ..... -0.3V to +15.0V
DC Supply Voltage (V0) ..... -0.3V to +15.0V
Input Voltage (Vin) ..... -0.3V to VDD+0.3V
Operating Ambient Temperature ..... -40°C to +85°C
Storage Temperature ..... -55°C to +125°C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device under these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

DC Characteristics (VSS = 0V, VDD = 1.8 ~ 3.6V, Ta = -40 ~ +85°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
VDD VDD3	Operating Voltage	1.8	-	3.6	V	
VDD2	Operating Voltage	1.8	-	3.6	V	2X, 3X boosting
		1.8	-	3.3		4X boosting
		1.8	-	2.8		5X boosting
VOUT	Booster Voltage	6.0	-	14.2	V	
V0	Voltage Regulator Operating Voltage	4.0	-	14.2	V	
VREG	Reference Voltage	**1.36**	**1.40**	**1.44**	V	Ta = 25°C, -0.05%/°C
IDD	Current Consumption	-	20	35	µA	VDD = 3V, V0 = 11V, built-in boosting power supply off, display on, display data = checker and no access, Ta = 25°C
		-	**120**	**160**	µA	VDD, VDD2 = 3V, V0 = 11V, 4X built-in boosting power supply, display on, display data = checker and no access, temperature gradient is -0.05%/ °C, Ta = 25°C, V0 voltage internal resistor is used, /HPM = 1 (normal power mode).
		-	**150**	**255**	µA	VDD, VDD2 = 3V, V0 = 11V, 4X built-in boosting power supply, display on, display data = checker and no access, temperature gradient is -0.05%/ °C, Ta = 25°C, V0 voltage internal resistor is used, /HPM = 0 (high power mode).

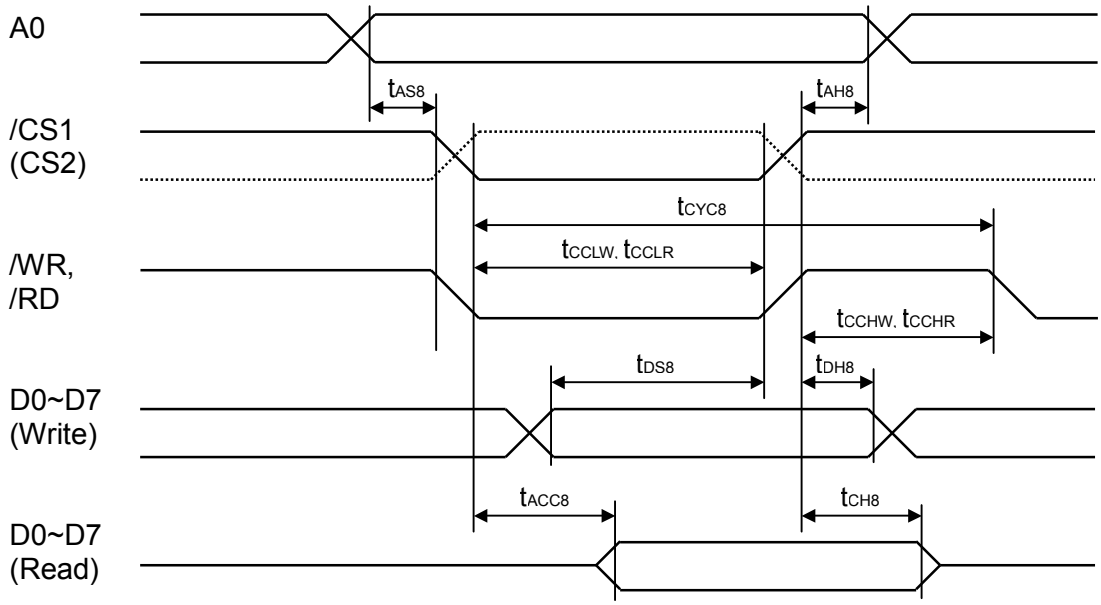
DC Characteristics (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
ISP	Sleep Mode Current Consumption	-	0.01	5	μA	During sleep, Ta = 25°C	
ISB	Standby Mode Current Consumption	-	4	8	μA	During standby, Ta = 25°C	
VIHC	High-Level Input Voltage	0.8 x VDD	-	VDD	V	A0, D0 - D7, /RD (E), /WR (R/W), /CS1, CS2, CLS, CL, FR, M/S, C86, P/S, /DOF, /RES, IRS and /HPM	
VILC	Low-Level Input Voltage	VSS	-	0.2 x VDD	V		
VOHC	High-Level Output Voltage	0.8 x VDD	-	VDD	V	IOH = -0.5mA (D0 - D7, FR, FRS, /DOF, and CL)	
VOLC	Low -Level Output Voltage	VDD	-	0.2 x VDD	V	IOL = 0.5mA (D0 - D7, FR, FRS, /DOF, and CL)	
ILI	Input Leakage Current	-1.0	-	1.0	μA	Vin = VDD or VSS (A0, /RD (E), /WR (R/W), /CS1, CS2, CLS, M/S, C86, P/S, IRS and /RES)	
IHZ	HZ Leakage Current	-3.0	-	3.0	μA	When the D0 - D7, FR, CL, and /DOF are in high impedance	
RON1	LCD Driver ON Resistance	-	2.0	3.5	KΩ	V0 = 11.0V	Ta = 25°C, These are the resistance values for when a 0.1V voltage is applied between the output terminals SEGn or COMn and the various power supply terminal (V0, V1, V2, V3, V4)
RON2	LCD Driver ON Resistance	-	3.2	5.4	KΩ	V0 = 8.0V	
CIN	Input Pad Capacity	-	5.0	8.0	pF	Ta = 25°C, f = 1MHz	
fFRM	Frame Frequency	78.0	80.5	83.0	Hz	fOSC = 31.4 KHz, 1/65duty VDD = 1.8~3.6V	
		64.9	67.4	69.9	Hz	fOSC = 26.3 KHz, 1/65duty VDD = 1.8~3.6V	

Notes: 1. Voltages V0 ≥ V1 ≥ V2 ≥ V3 ≥ V4 ≥ VSS2 must always be satisfied.

AC Characteristics

1. System Buses Read/Write Characteristics (for 8080 Series MPU)



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
T_{AH8}	Address hold time	0	-	-	ns	A0
T_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	240	-	-	ns	
t_{CCLW}	Control low pulse width (write)	90	-	-	ns	/WR
t_{CCLR}	Control low pulse width (read)	120	-	-	ns	/RD
t_{CCHW}	Control high pulse width (write)	100	-	-	ns	/WR
t_{CCHR}	Control high pulse width (read)	60	-	-	ns	/RD
T_{DS8}	Data setup time	**40**	-	-	ns	D0~D7
T_{DH8}	Data hold time	**0**	-	-	ns	
t_{ACC8}	/RD access time	-	-	140	ns	D0~D7, CL = 100pF
T_{CH8}	Output disable time	5	-	50	ns	

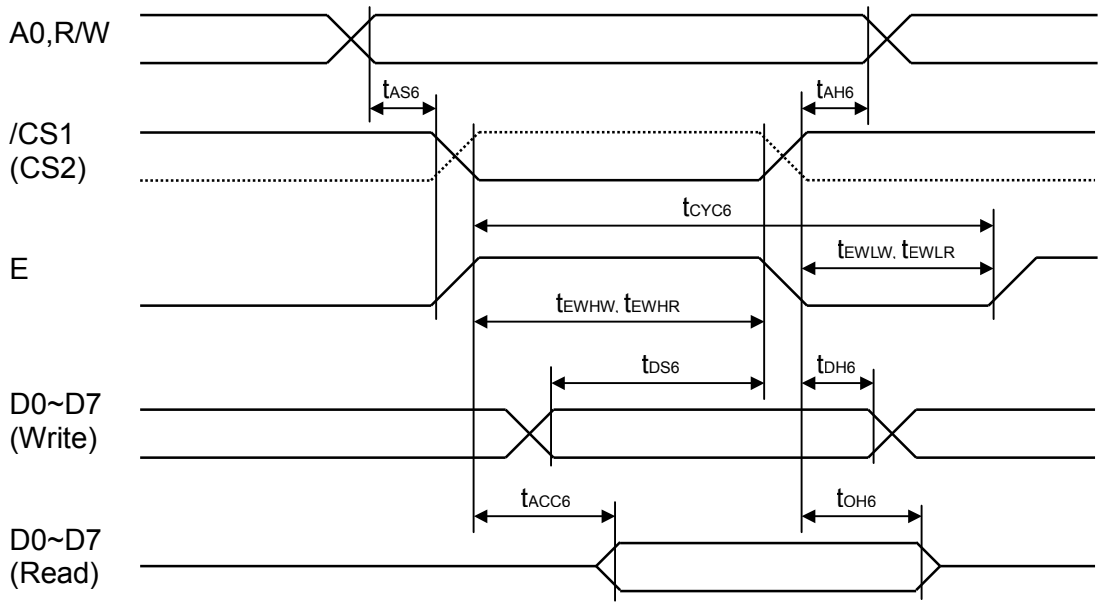
System Buses Read/Write Characteristics (for 8080 Series MPU) (continued)

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH8}	Address hold time	0	-	-	ns	A0
t_{AS8}	Address setup time	0	-	-	ns	
t_{CYC8}	System cycle time	400	-	-	ns	
t_{CCLW}	Control low pulse width (write)	150	-	-	ns	/WR
t_{CCLR}	Control low pulse width (read)	150	-	-	ns	/RD
t_{CCHW}	Control high pulse width (write)	120	-	-	ns	/WR
t_{CCHR}	Control high pulse width (read)	120	-	-	ns	/RD
t_{DS8}	Data setup time	80	-	-	ns	D0~D7
t_{DH8}	Data hold time	**0**	-	-	ns	
t_{ACC8}	/RD access time	-	-	240	ns	D0~D7, CL = 100pF
t_{CH8}	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < ($t_{CYC8} - t_{CCLW} - t_{CCHW}$) for write, ($t_r + t_f$) < ($t_{CYC8} - t_{CCLR} - t_{CCHR}$) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{CCLW} and t_{CCLR} are specified as the overlap interval when /CS1 is low (CS2 is high) and /WR or /RD is low.

2. System Buses Read/Write Characteristics (for 6800 Series MPU)



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH6}	Address hold time	0	-	-	ns	A0, R/W
t_{AS6}	Address setup time	0	-	-	ns	
t_{CYC6}	System cycle time	240	-	-	ns	
t_{EWHW}	Control high pulse width (write)	90	-	-	ns	E
t_{EWHR}	Control high pulse width (read)	120	-	-	ns	E
t_{EWLW}	Control low pulse width (write)	100	-	-	ns	E
t_{EWLR}	Control low pulse width (read)	60	-	-	ns	E
t_{DS6}	Data setup time	40	-	-	ns	D0~D7
t_{DH6}	Data hold time	0	-	-	ns	
t_{ACC6}	/RD access time	-	-	140	ns	D0~D7 CL = 100pF
t_{OH6}	Output disable time	5	-	50	ns	

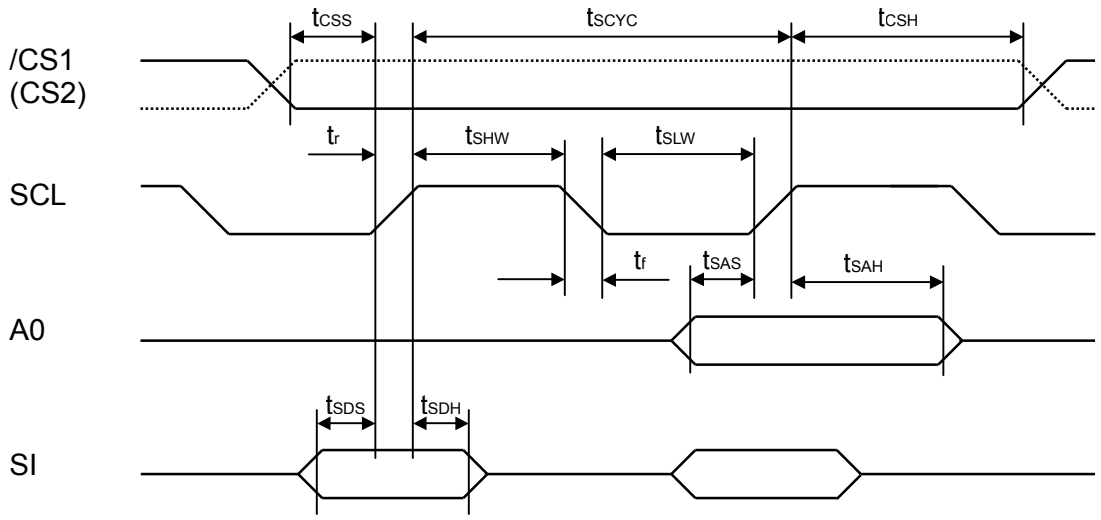
System Buses Read/Write Characteristics (for 6800 Series MPU) (continued)

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{AH6}	Address hold time	0	-	-	ns	A0, R/W
t_{AS6}	Address setup time	0	-	-	ns	
t_{CYC6}	System cycle time	400	-	-	ns	
t_{EWHW}	Control high pulse width (write)	150	-	-	ns	E
t_{EWHR}	Control high pulse width (read)	150	-	-	ns	E
t_{EWLW}	Control low pulse width (write)	120	-	-	ns	E
t_{EWLR}	Control low pulse width (read)	120	-	-	ns	E
t_{DS6}	Data setup time	80	-	-	ns	D0~D7
t_{DH6}	Data hold time	0	-	-	ns	
t_{ACC6}	/RD access time	-	-	240	ns	D0~D7 CL = 100pF
t_{OH6}	Output disable time	10	-	100	ns	

*1. The input signal rise time and fall time (t_r, t_f) is specified at 15ns or less.
($t_r + t_f$) < ($t_{CYC6} - t_{EWLW} - t_{EWHW}$) for write, ($t_r + t_f$) < ($t_{CYC6} - t_{EWLR} - t_{EWHR}$) for read.
*2. All timing is specified using 20% and 80% of VDD as the reference.
*3. t_{EWHW} and t_{EWHR} are specified as the overlap interval when /CS1 is low (CS2 is high) and E is high.

3. Serial Interface Timing



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	120	-	-	ns	SCL
t_{SHW}	Serial clock H pulse width	60	-	-	ns	SCL
t_{SLW}	Serial clock L pulse width	60	-	-	ns	SCL
t_{SAS}	Address setup time	30	-	-	ns	A0
t_{SAH}	Address hold time	20	-	-	ns	A0
t_{SDS}	Data setup time	30	-	-	ns	SI
t_{SDH}	Data hold time	**20**	-	-	ns	SI
t_{CSS}	Chip select setup time	20	-	-	ns	/CS1, CS2
t_{CSH}	Chip select hold time	40	-	-	ns	/CS1, CS2

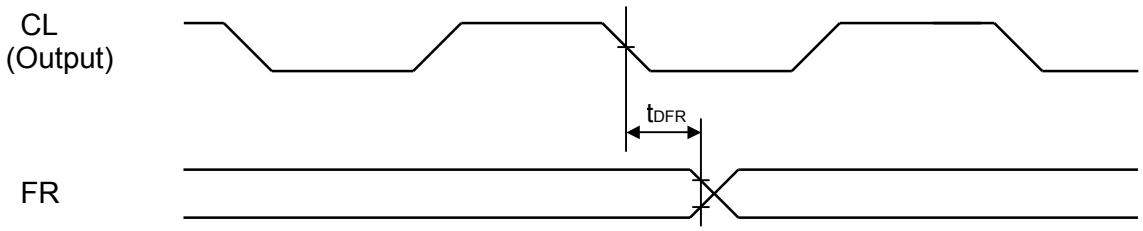
Serial Interface Timing (continued)

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{SCYC}	Serial clock cycle	200	-	-	ns	SCL
t_{SHW}	Serial clock H pulse width	80	-	-	ns	SCL
t_{SLW}	Serial clock L pulse width	80	-	-	ns	SCL
t_{SAS}	Address setup time	60	-	-	ns	A0
t_{SAH}	Address hold time	30	-	-	ns	A0
t_{SDS}	Data setup time	60	-	-	ns	SI
t_{SDH}	Data hold time	60	-	-	ns	SI
t_{CSS}	Chip select setup time	40	-	-	ns	/CS1, CS2
t_{CSH}	Chip select hold time	100	-	-	ns	/CS1, CS2

*1. The input signal rise time and fall time (t_r, t_f) is specified as 15ns or less.
*2. All timing is specified using 20% and 80% of VDD as the standard.

4. Display Control Timing



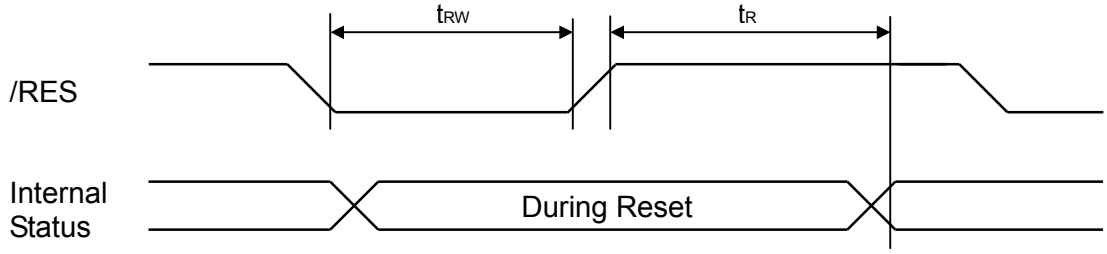
(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{DFR}	FR delay time	-	20	80	ns	CL = 50 pF

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{DFR}	FR delay time	-	40	160	ns	CL = 50 pF

5. Reset Timing



(VDD = 2.7 ~ 3.6V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset Time	-	-	1.0	µs	
t_{RW}	Reset low pulse width	10	-	-	µs	/RES

(VDD = 1.8 ~ 2.7V, Ta = -40 ~ +85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_R	Reset Time	-	-	2.0	µs	
t_{RW}	Reset low pulse width	20	-	-	µs	/RES

Microprocessor Interface (for reference only)

8080-series microprocessors

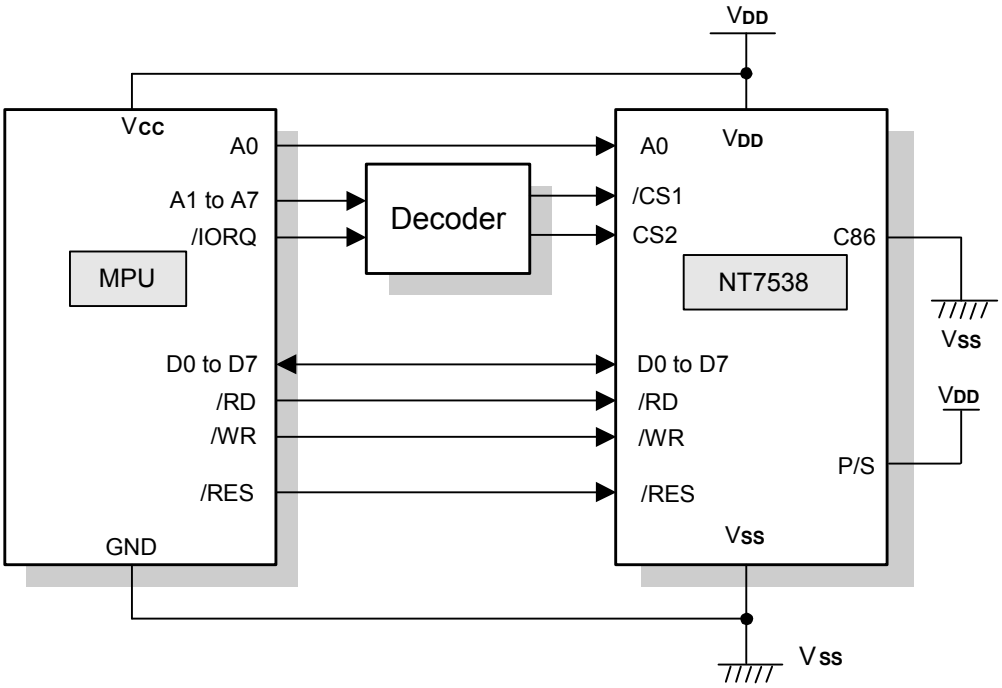


Figure 9

6800-series microprocessors

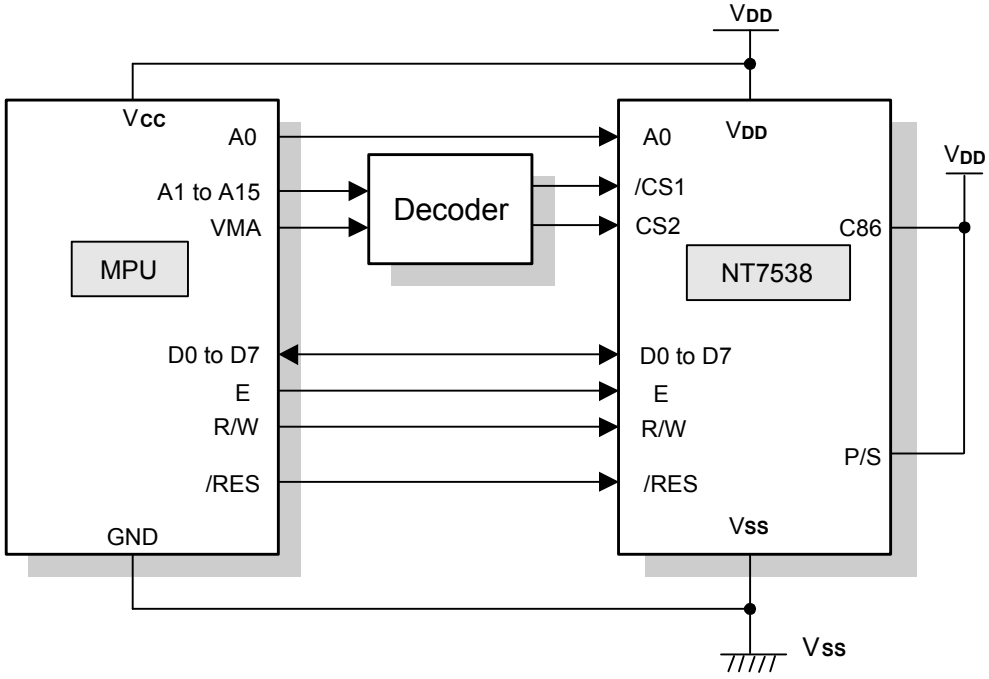


Figure 10

Connections between LCD Drivers (for reference only)

The liquid crystal display area can be enlarged with ease through the use of multiple NT7538 chips. Use same equipment type.

NT7538 (master) ↔ NT7538 (slave)

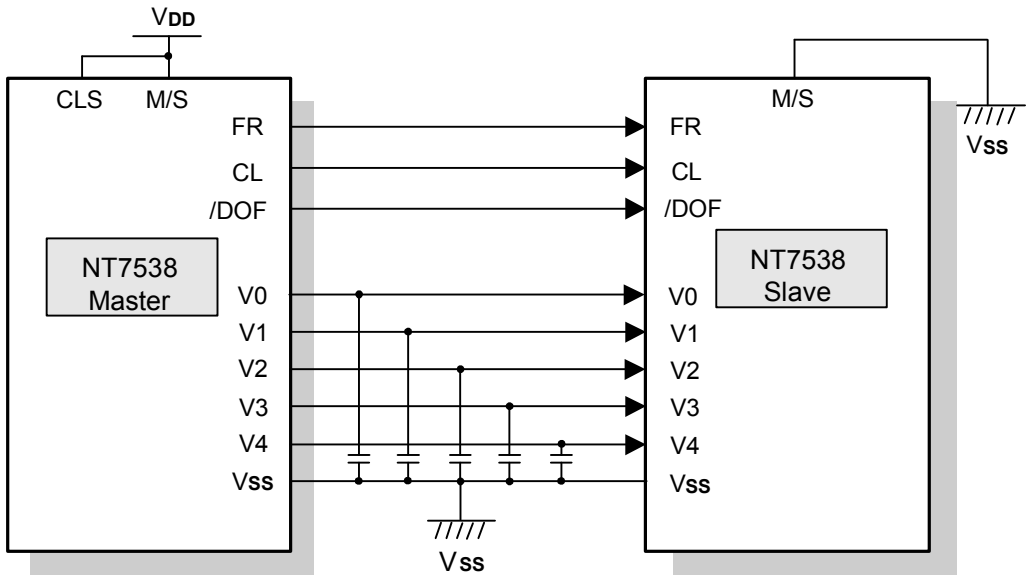
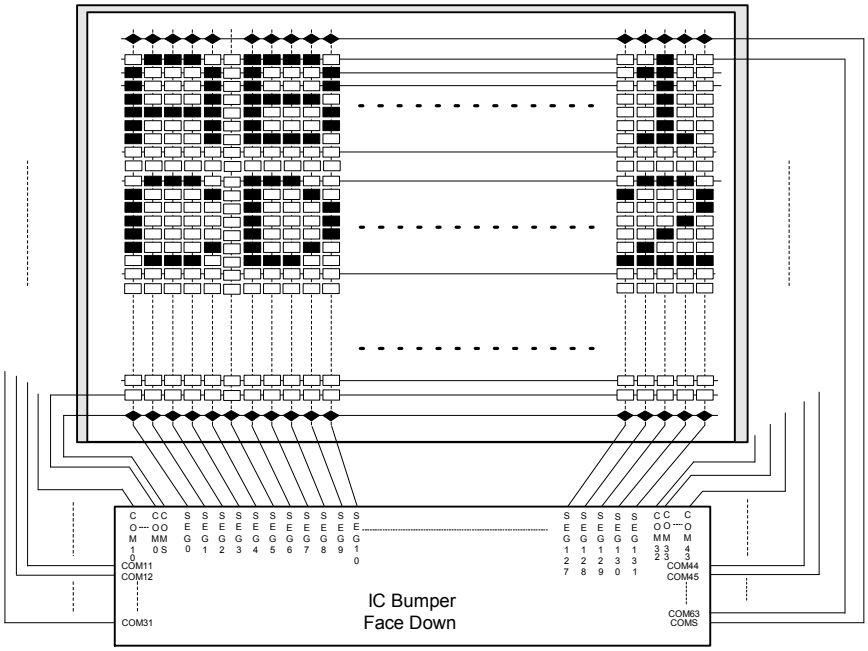


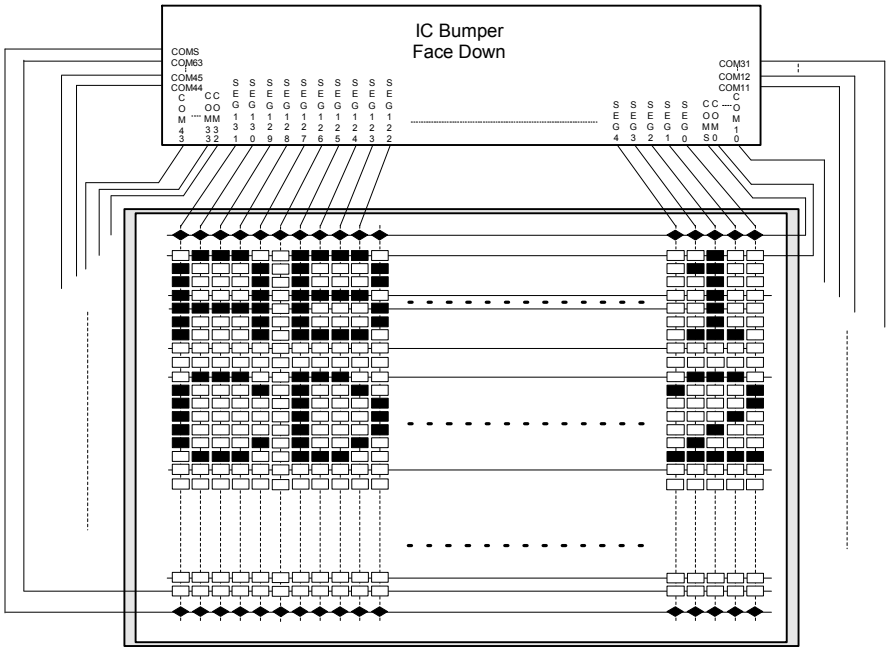
Figure 11

Application information for LCD panel (for reference only)

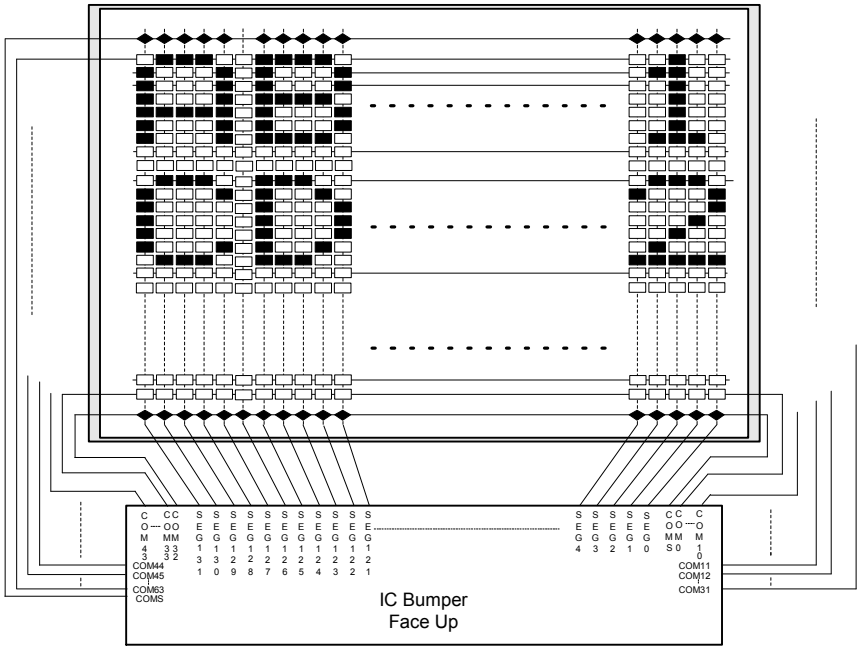
1. Type I (ADC Select = 0, COM Output Select = 1)



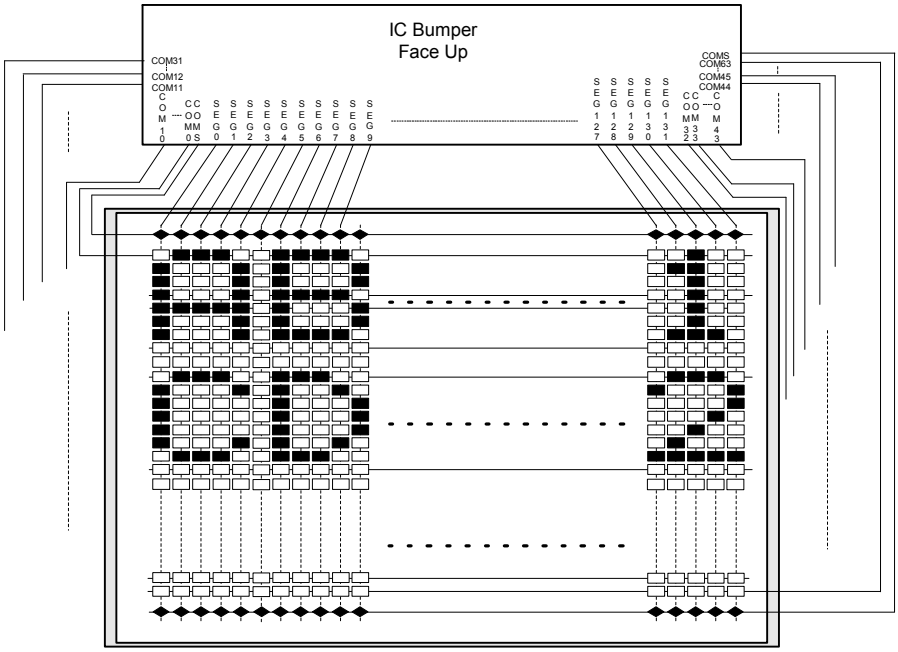
2. Type II (ADC Select = 1, COM Output Select = 0)



3. Type III (ADC Select = 1, COM Output Select = 1)

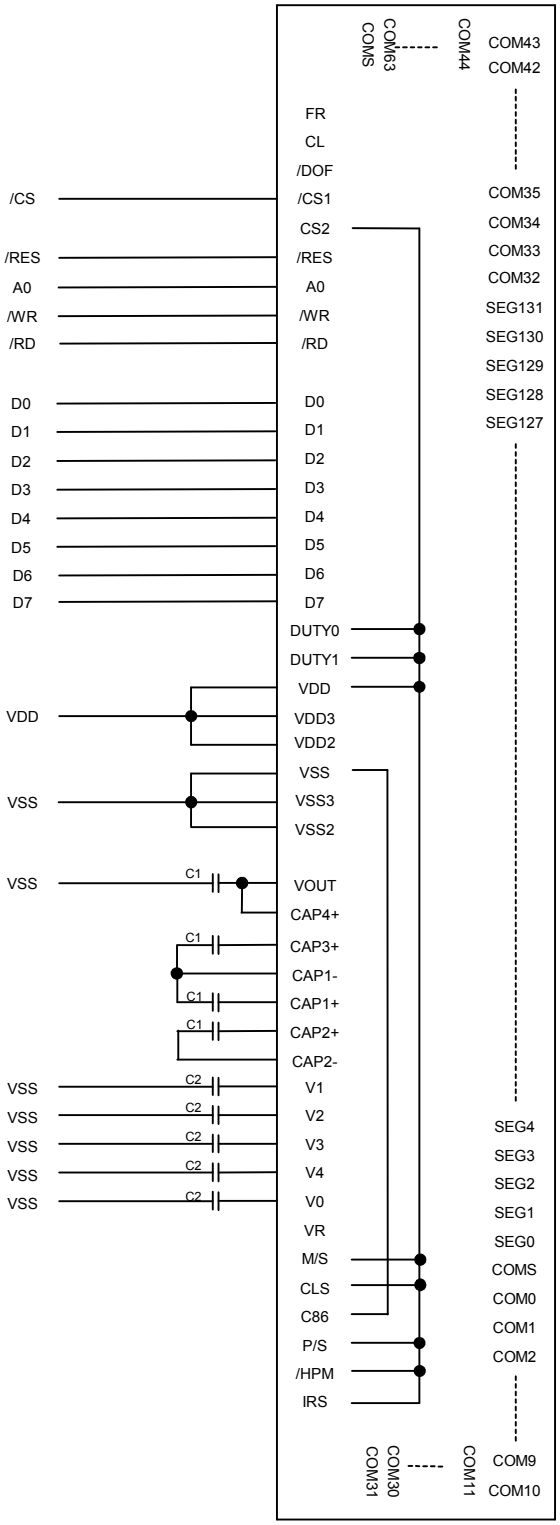


4. Type IV (ADC Select = 0, COM Output Select = 0)

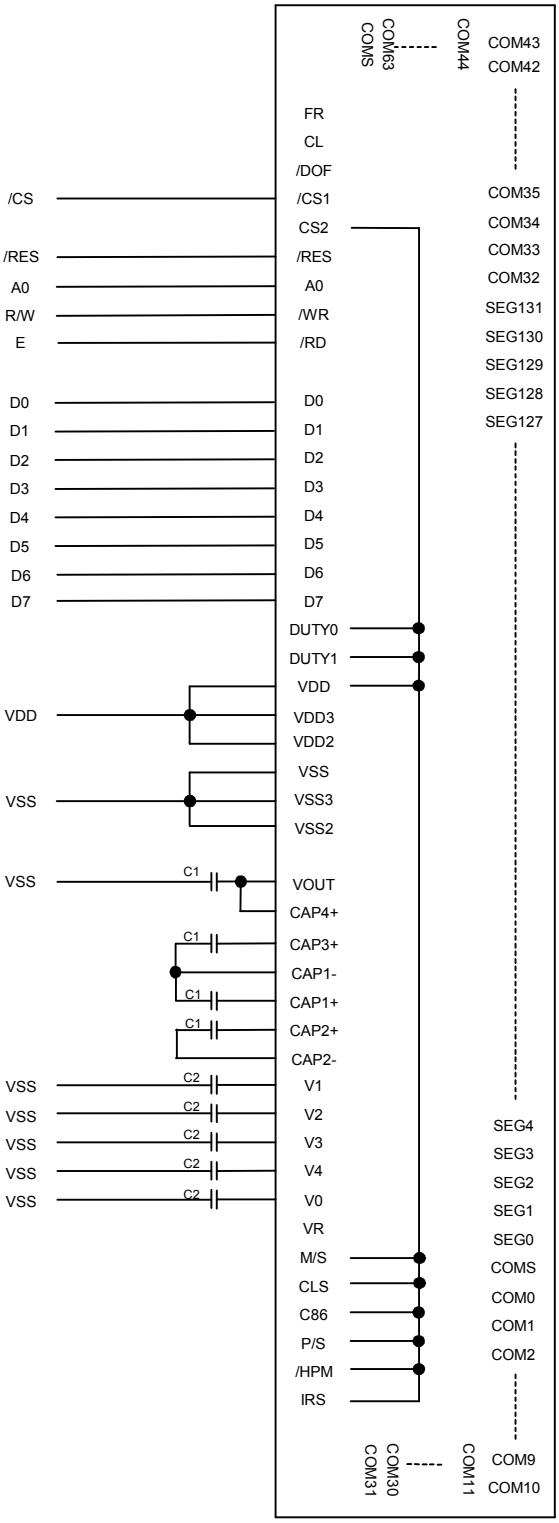


Application information for Pin Connection to MPU (for reference only)

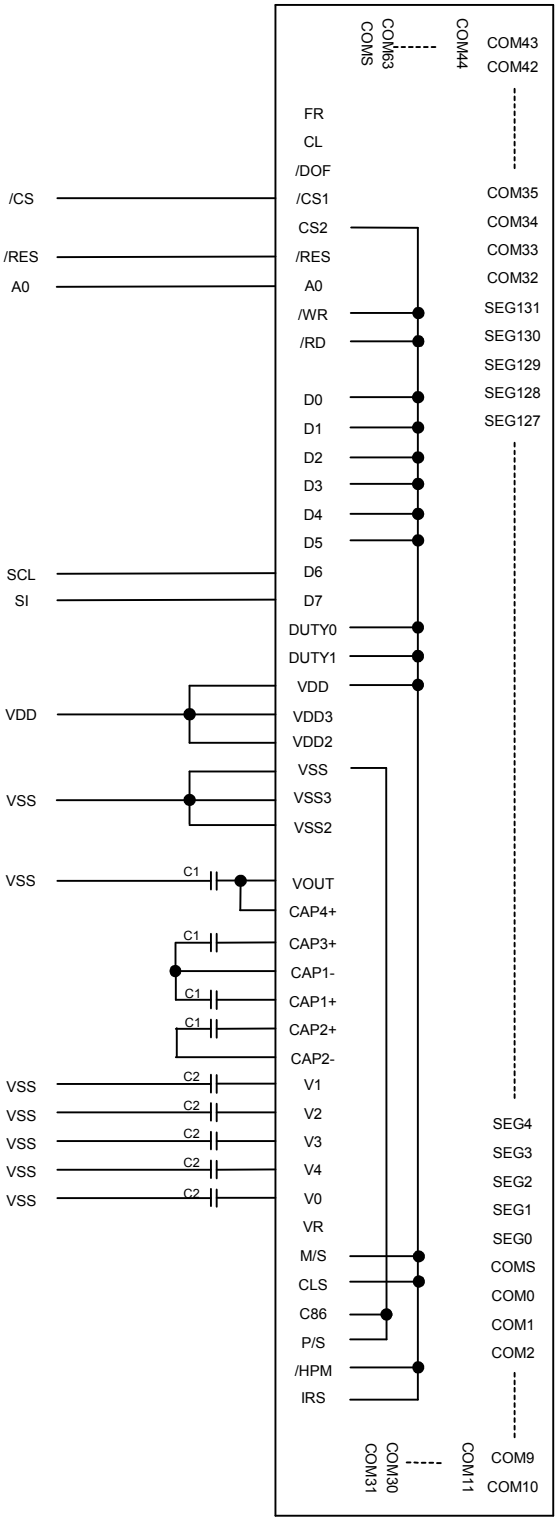
1. 8080 MPU Mode: (DUTY0,1 = 11: 1/65duty, M/S = 1: Master mode, CLS = 1: Internal display OSC, /HPM = 1: Normal power mode, IRS = 1: Internal Rb/Ra)



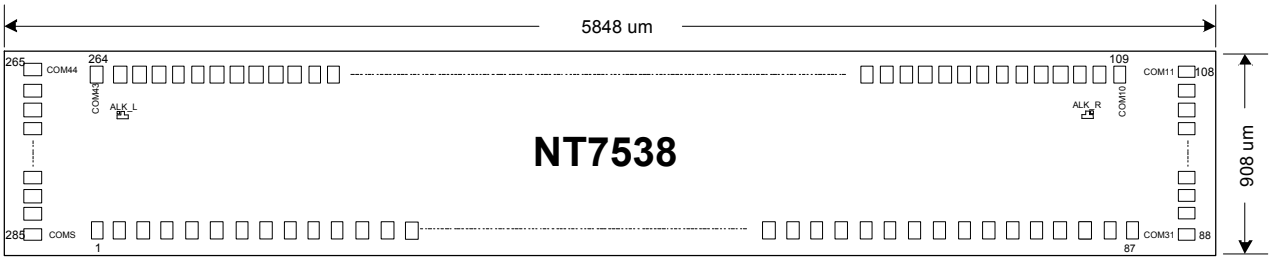
2. 6800 MPU Mode: (DUTY0,1 = 11: 1/65duty, M/S = 1: Master mode, CLS = 1: Internal display OSC, /HPM = 1: Normal power mode, IRS = 1: Internal Rb/Ra)



3. Serial Mode: (DUTY0,1 = 11: 1/65duty, M/S = 1: Master mode, CLS = 1: Internal display OSC, /HPM = 1: Normal power mode, IRS = 1: Internal Rb/Ra)



Bonding Diagram



Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
1	FRS	-2610.00	-340.00	30	DUTY0	-810.00	-340.00
2	FR	-2550.00	-340.00	31	VSS	-750.00	-340.00
3	CL	-2490.00	-340.00	32	DUTY1	-690.00	-340.00
4	/DOF	-2430.00	-340.00	33	VCC	-630.00	-340.00
5	VSS	-2370.00	-340.00	34	VCC	-570.00	-340.00
6	/CS1	-2310.00	-340.00	35	VCC	-510.00	-340.00
7	CS2	-2250.00	-340.00	36	VDD3	-450.00	-340.00
8	VDD	-2190.00	-340.00	37	VDD2	-390.00	-340.00
9	/RES	-2070.00	-340.00	38	VDD2	-330.00	-340.00
10	A0	-2010.00	-340.00	39	VDD2	-270.00	-340.00
11	/WR	-1950.00	-340.00	40	GND	-210.00	-340.00
12	/RD	-1890.00	-340.00	41	GND	-150.00	-340.00
13	VDD	-1830.00	-340.00	42	GND	-90.00	-340.00
14	D0	-1770.00	-340.00	43	VSS3	-30.00	-340.00
15	D0	-1710.00	-340.00	44	VSS2	30.00	-340.00
16	D1	-1650.00	-340.00	45	VSS2	90.00	-340.00
17	D1	-1590.00	-340.00	46	VSS2	150.00	-340.00
18	D2	-1530.00	-340.00	47	VOUT	210.00	-340.00
19	D2	-1470.00	-340.00	48	VOUT	270.00	-340.00
20	D3	-1410.00	-340.00	49	VOUT	330.00	-340.00
21	D3	-1350.00	-340.00	50	CP4	390.00	-340.00
22	D4	-1290.00	-340.00	51	CP4	450.00	-340.00
23	D4	-1230.00	-340.00	52	CP4	510.00	-340.00
24	D5	-1170.00	-340.00	53	CP3	570.00	-340.00
25	D5	-1110.00	-340.00	54	CP3	630.00	-340.00
26	D6	-1050.00	-340.00	55	CP3	690.00	-340.00
27	D6	-990.00	-340.00	56	CN1	750.00	-340.00
28	D7	-930.00	-340.00	57	CN1	810.00	-340.00
29	D7	-870.00	-340.00	58	CN1	870.00	-340.00

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
59	CP1	930.00	-340.00	95	COM24	2790.00	-102.00
60	CP1	990.00	-340.00	96	COM23	2790.00	-68.00
61	CP1	1050.00	-340.00	97	COM22	2790.00	-34.00
62	CP2	1110.00	-340.00	98	COM21	2790.00	0.00
63	CP2	1170.00	-340.00	99	COM20	2790.00	34.00
64	CP2	1230.00	-340.00	100	COM19	2790.00	68.00
65	CN2	1290.00	-340.00	101	COM18	2790.00	102.00
66	CN2	1350.00	-340.00	102	COM17	2790.00	136.00
67	CN2	1410.00	-340.00	103	COM16	2790.00	170.00
68	V1	1470.00	-340.00	104	COM15	2790.00	204.00
69	V1	1530.00	-340.00	105	COM14	2790.00	238.00
70	V2	1590.00	-340.00	106	COM13	2790.00	272.00
71	V2	1650.00	-340.00	107	COM12	2790.00	306.00
72	V3	1710.00	-340.00	108	COM11	2790.00	340.00
73	V3	1770.00	-340.00	109	COM10	2635.00	320.00
74	V4	1830.00	-340.00	110	COM9	2601.00	320.00
75	V4	1890.00	-340.00	111	COM8	2567.00	320.00
76	V0	1950.00	-340.00	112	COM7	2533.00	320.00
77	V0	2010.00	-340.00	113	COM6	2499.00	320.00
78	VR	2070.00	-340.00	114	COM5	2465.00	320.00
79	VDD	2130.00	-340.00	115	COM4	2431.00	320.00
80	M/S	2190.00	-340.00	116	COM3	2397.00	320.00
81	CLS	2250.00	-340.00	117	COM2	2363.00	320.00
82	C86	2310.00	-340.00	118	COM1	2329.00	320.00
83	VSS	2370.00	-340.00	119	COM0	2295.00	320.00
84	PS	2430.00	-340.00	120	COMS	2261.00	320.00
85	/HPM	2490.00	-340.00	121	SEG0	2227.00	320.00
86	IRS	2550.00	-340.00	122	SEG1	2193.00	320.00
87	VDD	2610.00	-340.00	123	SEG2	2159.00	320.00
88	COM31	2790.00	-340.00	124	SEG3	2125.00	320.00
89	COM30	2790.00	-306.00	125	SEG4	2091.00	320.00
90	COM29	2790.00	-272.00	126	SEG5	2057.00	320.00
91	COM28	2790.00	-238.00	127	SEG6	2023.00	320.00
92	COM27	2790.00	-204.00	128	SEG7	1989.00	320.00
93	COM26	2790.00	-170.00	129	SEG8	1955.00	320.00
94	COM25	2790.00	-136.00	130	SEG9	1921.00	320.00

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
131	SEG10	1887.00	320.00	167	SEG46	663.00	320.00
132	SEG11	1853.00	320.00	168	SEG47	629.00	320.00
133	SEG12	1819.00	320.00	169	SEG48	595.00	320.00
134	SEG13	1785.00	320.00	170	SEG49	561.00	320.00
135	SEG14	1751.00	320.00	171	SEG50	527.00	320.00
136	SEG15	1717.00	320.00	172	SEG51	493.00	320.00
137	SEG16	1683.00	320.00	173	SEG52	459.00	320.00
138	SEG17	1649.00	320.00	174	SEG53	425.00	320.00
139	SEG18	1615.00	320.00	175	SEG54	391.00	320.00
140	SEG19	1581.00	320.00	176	SEG55	357.00	320.00
141	SEG20	1547.00	320.00	177	SEG56	323.00	320.00
142	SEG21	1513.00	320.00	178	SEG57	289.00	320.00
143	SEG22	1479.00	320.00	179	SEG58	255.00	320.00
144	SEG23	1445.00	320.00	180	SEG59	221.00	320.00
145	SEG24	1411.00	320.00	181	SEG60	187.00	320.00
146	SEG25	1377.00	320.00	182	SEG61	153.00	320.00
147	SEG26	1343.00	320.00	183	SEG62	119.00	320.00
148	SEG27	1309.00	320.00	184	SEG63	85.00	320.00
149	SEG28	1275.00	320.00	185	SEG64	51.00	320.00
150	SEG29	1241.00	320.00	186	SEG65	17.00	320.00
151	SEG30	1207.00	320.00	187	SEG66	-17.00	320.00
152	SEG31	1173.00	320.00	188	SEG67	-51.00	320.00
153	SEG32	1139.00	320.00	189	SEG68	-85.00	320.00
154	SEG33	1105.00	320.00	190	SEG69	-119.00	320.00
155	SEG34	1071.00	320.00	191	SEG70	-153.00	320.00
156	SEG35	1037.00	320.00	192	SEG71	-187.00	320.00
157	SEG36	1003.00	320.00	193	SEG72	-221.00	320.00
158	SEG37	969.00	320.00	194	SEG73	-255.00	320.00
159	SEG38	935.00	320.00	195	SEG74	-289.00	320.00
160	SEG39	901.00	320.00	196	SEG75	-323.00	320.00
161	SEG40	867.00	320.00	197	SEG76	-357.00	320.00
162	SEG41	833.00	320.00	198	SEG77	-391.00	320.00
163	SEG42	799.00	320.00	199	SEG78	-425.00	320.00
164	SEG43	765.00	320.00	200	SEG79	-459.00	320.00
165	SEG44	731.00	320.00	201	SEG80	-493.00	320.00
166	SEG45	697.00	320.00	202	SEG81	-527.00	320.00

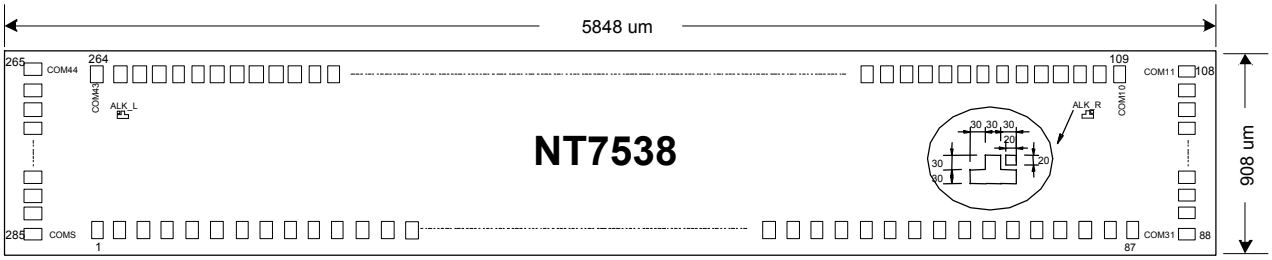
Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
203	SEG82	-561.00	320.00	239	SEG118	-1785.00	320.00
204	SEG83	-595.00	320.00	240	SEG119	-1819.00	320.00
205	SEG84	-629.00	320.00	241	SEG120	-1853.00	320.00
206	SEG85	-663.00	320.00	242	SEG121	-1887.00	320.00
207	SEG86	-697.00	320.00	243	SEG122	-1921.00	320.00
208	SEG87	-731.00	320.00	244	SEG123	-1955.00	320.00
209	SEG88	-765.00	320.00	245	SEG124	-1989.00	320.00
210	SEG89	-799.00	320.00	246	SEG125	-2023.00	320.00
211	SEG90	-833.00	320.00	247	SEG126	-2057.00	320.00
212	SEG91	-867.00	320.00	248	SEG127	-2091.00	320.00
213	SEG92	-901.00	320.00	249	SEG128	-2125.00	320.00
214	SEG93	-935.00	320.00	250	SEG129	-2159.00	320.00
215	SEG94	-969.00	320.00	251	SEG130	-2193.00	320.00
216	SEG95	-1003.00	320.00	252	SEG131	-2227.00	320.00
217	SEG96	-1037.00	320.00	253	COM32	-2261.00	320.00
218	SEG97	-1071.00	320.00	254	COM33	-2295.00	320.00
219	SEG98	-1105.00	320.00	255	COM34	-2329.00	320.00
220	SEG99	-1139.00	320.00	256	COM35	-2363.00	320.00
221	SEG100	-1173.00	320.00	257	COM36	-2397.00	320.00
222	SEG101	-1207.00	320.00	258	COM37	-2431.00	320.00
223	SEG102	-1241.00	320.00	259	COM38	-2465.00	320.00
224	SEG103	-1275.00	320.00	260	COM39	-2499.00	320.00
225	SEG104	-1309.00	320.00	261	COM40	-2533.00	320.00
226	SEG105	-1343.00	320.00	262	COM41	-2567.00	320.00
227	SEG106	-1377.00	320.00	263	COM42	-2601.00	320.00
228	SEG107	-1411.00	320.00	264	COM43	-2635.00	320.00
229	SEG108	-1445.00	320.00	265	COM44	-2790.00	340.00
230	SEG109	-1479.00	320.00	266	COM45	-2790.00	306.00
231	SEG110	-1513.00	320.00	267	COM46	-2790.00	272.00
232	SEG111	-1547.00	320.00	268	COM47	-2790.00	238.00
233	SEG112	-1581.00	320.00	269	COM48	-2790.00	204.00
234	SEG113	-1615.00	320.00	270	COM49	-2790.00	170.00
235	SEG114	-1649.00	320.00	271	COM50	-2790.00	136.00
236	SEG115	-1683.00	320.00	272	COM51	-2790.00	102.00
237	SEG116	-1717.00	320.00	273	COM52	-2790.00	68.00
238	SEG117	-1751.00	320.00	274	COM53	-2790.00	34.00

Pad No.	Designation	X	Y	Pad No.	Designation	X	Y
275	COM54	-2790.00	0.00	281	COM60	-2790.00	-204.00
276	COM55	-2790.00	-34.00	282	COM61	-2790.00	-238.00
277	COM56	-2790.00	-68.00	283	COM62	-2790.00	-272.00
278	COM57	-2790.00	-102.00	284	COM63	-2790.00	-306.00
279	COM58	-2790.00	-136.00	285	COMS	-2790.00	-340.00
280	COM59	-2790.00	-170.00				

Alignment Mark Location (Total: 2 pins)

NO	X	Y
L	-2514.00	107.00
R	2514.00	107.00

Package Information



Pad Dimensions

Item	Pad No.		Size		Unit
			X	Y	
Chip size	-		5848	908	μm
Chip thickness	-		525		μm
Pad pitch	1~8, 10~87		60		μm
	88~285		34		
	8~9		120		
Bump size	Output Pad	88~108, 265~285	110	19	μm
		109~264	19	110	
	Input Pad	1~87	42	70	
Bump height	All pads		15 ± 3		μm

Ordering Information

Part No.	Packages
NT7538H-BDT	Gold Bump on Chip Tray

Cautions

1. The contents of this document will be subjected to change without notice.
2. Precautions against light projection:
   Light has the effect of causing the electrons of semiconductor to move; so light projection may change the characteristics of semiconductor devices. For this reason, it is necessary to take account of effective protection measures for the packages (such as COB and COG, etc.) causing chip to be exposed to a light environment in order to isolate the projection of light on any part of the chip, including top, bottom and the area around the chip.
   Observe the following instructions in using this product:
   a. During the design stage, it is necessary to notice and confirm the light sensitivity and preventive measures for using IC on substrate (PCB, Glass or Film) or product.
   b. Test and inspect the product under an environment free of light source penetration.
   c. Confirm that all surfaces around the IC will not be exposed to light source.